

II

Converter Microcircuits

Chapter II-2

As the use of digital techniques in measurement, communication, and control grew by leaps and bounds, the size and price of processors and other LSI (and MSI) logic shrank in similar degree, with the inevitable result that further penetration of digital techniques into those fields became inevitable, in the regenerative fashion that is characteristic of the integrated-circuit era. Along with such other peripherals as keyboards, displays, and memories, converters have followed this spiralling trend — as a matter of necessity.

But it hasn't been easy. Linear IC's have always been more difficult to fabricate for reasonable degrees of resolution and accuracy than digital IC's — in part because the variables that are the input or output involve a continuum of voltage or current, rather than the easier-to-handle two-valued logic. While the problems of implementing digital circuitry have involved questions of functions-per-chip, speed, and dissipation, the analog (precision IC) problems have related more to simple existence and survival. Such matters as offset, bias current, drift, dynamic stability, common-mode errors, and open-loop gain — as well as slewing rate and settling time — have concerned both designers and users of op amps (the “representative” linear-IC product). And op amps entered the “commodity-IC” era a good deal later than (for example) TTL logic.

But converters are more difficult by at least an order-of-magnitude. While IC op amps called for precision transistor circuitry and clever design, and IC analog multipliers added a need for precision resistors (and references) — but to-date have attained accuracies to within 0.1% (at best) and are hardly in the commodity class — *converters* call for all of these prodigies of linear design and processing, and *more*: on-chip switches, logic, and everyday resolutions of from 10 to 12 bits (corresponding to accuracies-to-within 0.05% to 0.0125%).

Although the technology still has a considerable distance to go, it is worthwhile to consider the progress made, just within the past five years, as measured by entries within the Analog Devices catalog. In the 1972 *Product Guide*, the IC conversion Product Line consisted of just two families of monolithic quad switches (and compatible resistor networks) for constructing precision 8-10-12 bit A/D and D/A converters, using the design approach described in Chapter II-3. In the just-published 1977 *Short-Form Guide*, there are 12 *families* of IC A/D and D/A converters, spanning resolutions from 8 to 13 bits and technologies from laser-trimmed-on-the-wafer bipolar to thin-films-on-CMOS to hybrids. They include 4-quadrant multiplying DAC's, microprocessor-compatible ADC's and DAC's, and high resolution-and-accuracy devices. And, in addition, there is a large supporting cast of monolithic conversion-related products, including references, sample-holds, multiplexers, CMOS switches, resistance networks, and V/F converters.

The perceptive Reader will observe that such a wealth of products would not be possible if the difficulties due to the diversity of circuitry required on a single chip outweighed the advantages of monolithic IC construction. And indeed, there are significant advantages: components that must be well-matched are inherently well-matched; the small size of the chip makes for excellent thermal tracking; and the low-cost per-die on a reasonably high-yielding wafer results in an attractive price for the end-product, which is welcomed by the user because of both low cost and small size.

TECHNOLOGIES FOR CONVERTERS

As Chapter II-1 points out, the complete D/A converter comprises the basic resistance network and set of switches, plus a reference (if required), registers (if required), current sources (if required), and an output op amp (if voltage output is required). A/D converter circuit requirements depend on the design approach. Integrating types require integrators and counters; successive-approximation types require DAC's and successive-approximation registers; both types need comparators, clocks, and control logic — and they may need references and three-state output registers.

Different technologies are used to optimize devices in production to meet differing classes of user needs (and to accommodate the current state of the Art). It may be useful to discuss these considerations in terms of their application to existing devices now in production and on the market (tabulated in Chapter II-5) and to look briefly into the likely short-term future.

- *CMOS and the AD7520.* CMOS excels at low-power high-density digital logic circuitry and analog voltage switches. It isn't very suitable for high-performance linear circuitry. The AD7520 — and its close relatives, the AD7530 and the 12-bit AD7521 & AD7531 — contain CMOS switches with graduated R_{on} and the logic to drive them (Figure 1), and a thin-film-on-the-chip R-2R ladder network (a significant advance in the technology). The result (to be discussed in detail later) is a digitally controlled attenuator, with 8-10-12-bit conversion-linearity and even better inherent analog-linearity, with very low feedthrough, to frequencies beyond 50kHz. Besides ordinary converter applications, it has many uses as a 2- or 4-quadrant multiplying DAC and as a "digital pot." However, it does require an external op amp, a reference (if used in fixed-reference applications), and registers (if it must interface with processors).

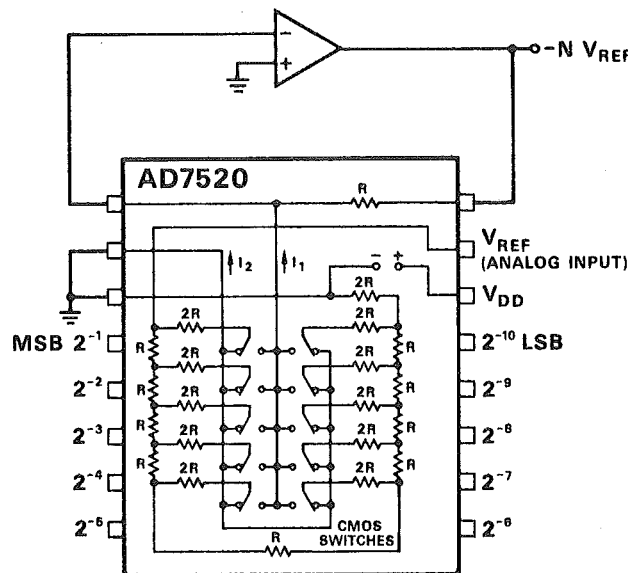


Figure 1. AD7520 10-bit DAC.

- *More CMOS — the AD7522.* The AD7522, using the compact-logic capability of CMOS, provides — not just one, but — *two* sets of registers, together with the switches and resistors of the AD7520. The result is a double-buffered DAC (Figure 2) that can be directly interfaced to a microprocessor for byte-serial updating. For example, the 8 bits in the low byte can be latched into the buffer register, then the 2 bits in the high byte, and then the whole digital word can be latched into the DAC register to update the analog output at once. The AD7522 also accepts (and shifts along) serial data. And (of course) the input latches can be updated in parallel. An external reference and an output amplifier are still needed for many applications, but the freedom to choose the characteristics of both the reference and the output amplifier is often a great advantage.

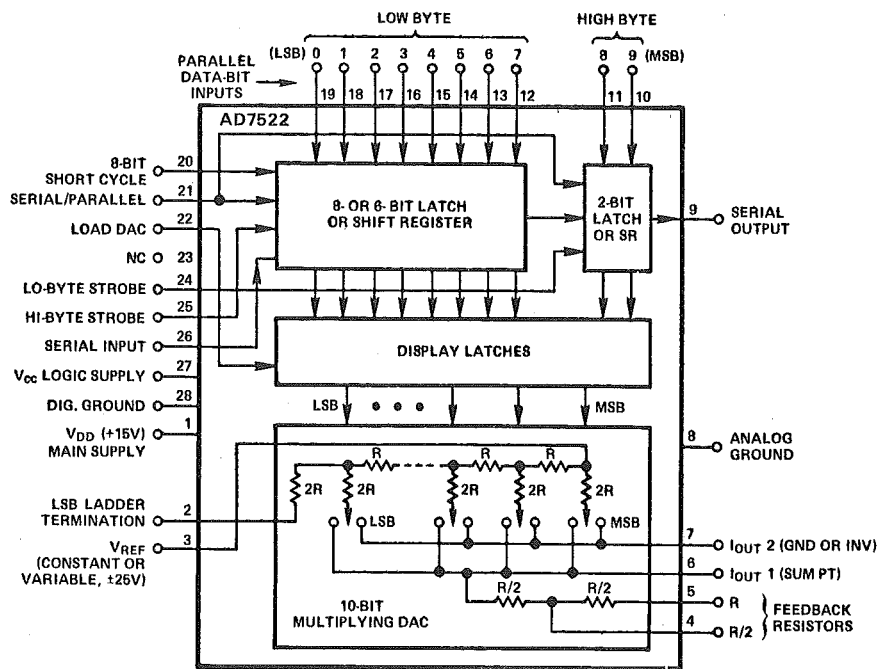


Figure 2. Functional diagram of the AD7522.

• **CMOS A/D Conversion – the AD7570.** The AD7570 is a 10-bit successive-approximation A/D converter that requires only an external reference and a comparator. As Figure 3 shows, it contains a D/A converter (much like the AD7520), control logic, a successive-approximations register, and a three-state output register, that comprises two bytes, for compatibility with micro-processors. The conversion can be self-clocked or driven by an external clock. Since the reference is external, ratiometric conversion is inherent.

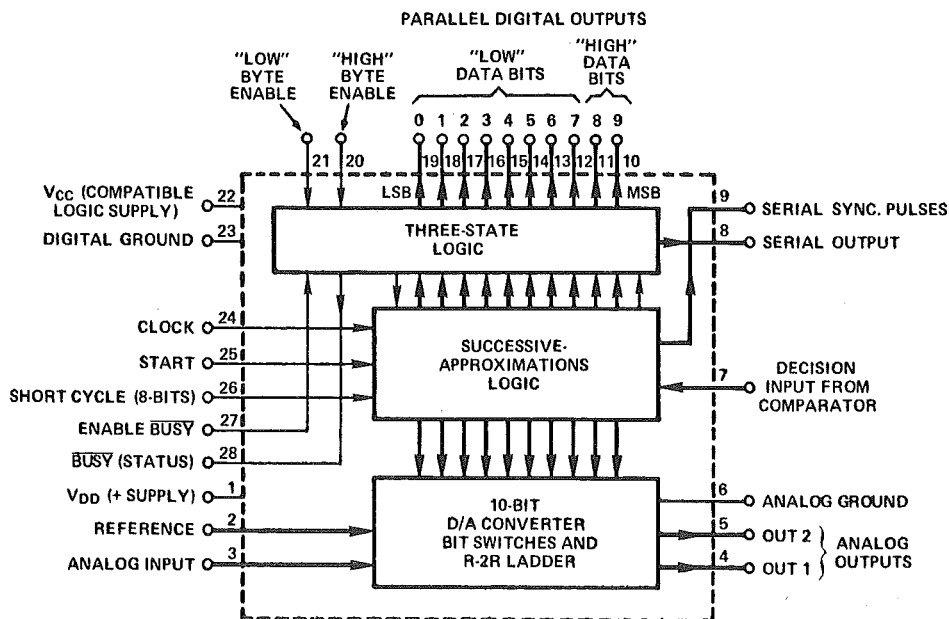


Figure 3. AD7570 10-bit A/D converter.

• **CMOS Quad-Slope Conversion - the AD7550.** The difficulties faced by CMOS in handling analog signals with precision are overcome by integrating-conversion employing “quad slope.” *The AD7550 (Figure 4) contains an integrating amplifier, a comparator, timing and control logic, and counters. Two cycles of dual-slope integration occur – in the first, analog ground is measured against the reference; any errors introduced by the amplifier

*U.S. Patent 3,872,466.

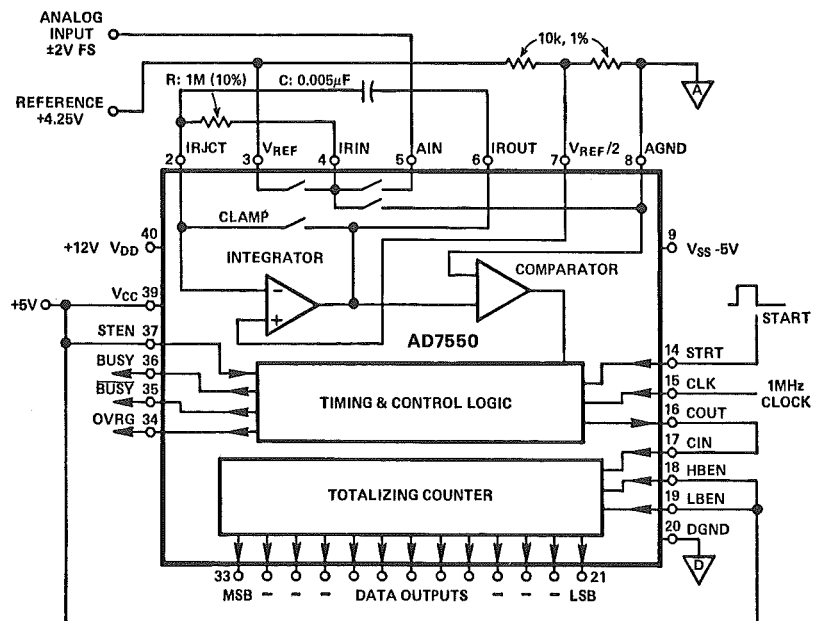


Figure 4. AD7550 connections for basic operation.

and the comparator are stored as a digital count. In the second cycle, the input voltage is measured against the reference, and the error count is subtracted from the output count. (This process will be discussed in greater detail later.)

The technique is very effective: 13-bit conversion occurs, with tempcos in the neighborhood of 1ppm/°C. The only external components needed are the integrating R-C and a (not-very-precise) voltage divider. Data are available in two bytes that can be separately enabled, for interfacing with 8-bit microprocessors. (Since integrating-type conversions require many milliseconds, the status-enable avoids tying-up the processor; end-of-conversion (EOC) can be checked by a polling routine at a time when it is reasonably certain, or on an interrupt basis, for greatest speed.)

● *Bipolar Conversion – the AD562 DAC.* Until the recent developments in Integrated Injection Logic (I²L), reasonably fast IC logic circuitry called for low-voltage processing, and reasonably accurate circuitry (compatible with analog electronics) called for a higher-voltage process, two requirements that were mutually exclusive. The AD562 was an early example of a happy combination of technologies for stable, linear, reasonably fast 12-bit D/A conversion, in which clever circuit-design compensated to some extent for process limitations.

As the functional block diagram in Figure 5 shows, the AD562 consists of a resistance-network chip (laser-trimmed in actual operation) and a complementary amplifier-and-switch chip, embodying (in effect) three sets of quad switches. Unlike the essentially passive AD7520 CMOS species, the AD562 is an *active* device; the reference voltage is transduced to a current, and the output current is a reflected version of it, with the relative magnitude a function of the digital code.

Aspects of the design that contribute to 12-bit (and better) linearity, with microsecond settling, include scaled emitter areas for equal and tracking V_{be} 's, a reference transistor and control amplifier, and current-steering switches that, switching at constant voltage, do not require time-consuming charge transfer. These matters will be discussed later. The external reference can be chosen for desired absolute-accuracy characteristics, and the external op amp can be chosen on the basis of desired output speed.

● *Bipolar Conversion – the AD561 DAC.* This is a monolithic 10-bit converter with an internal reference and high-compliance current output. A number of advanced technologies are combined to provide outstanding performance: the resistance network is a silicon-chromium R-2R ladder deposited directly on the chip and laser-trimmed at the *wafer-probe*

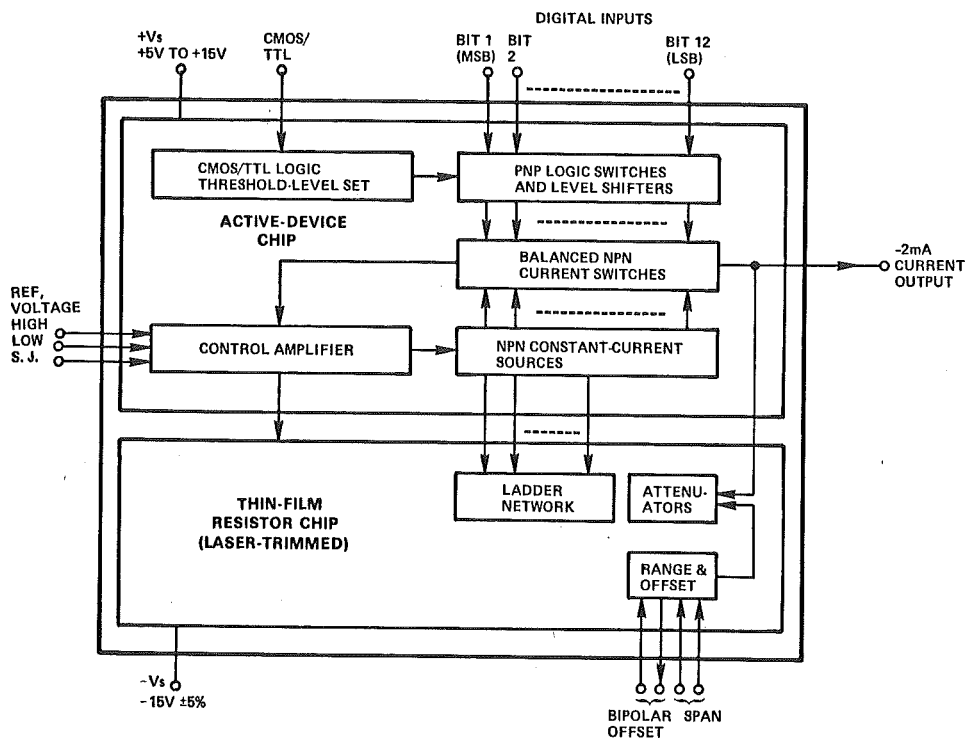


Figure 5. Functional block diagram of the AD562.

stage. The reference is a *buried* Zener diode with high stability – a consequence of its freedom from surface effects.

Because the current-setting network is an R-2R ladder (Figure 6), the output switches do not require attenuation-while-summing of lower-order quad currents, hence the output impedance is of the order of $40M\Omega$, and the usable compliance-voltage range is from $-2V$ to $+10V$ (a simple calculation will show that a swing through the entire compliance range will cause an error of less than 0.2 LSB). This permits a direct voltage output, with an arbitrary load resistance, or direct current-summing at the comparator when the AD561 is used in an ADC circuit. Of course, a conventional output op amp may also be used, chosen for the desired speed of voltage-settling – the converter itself has a 250ns current-settling-time to within $\pm\frac{1}{2}$ LSB, and a 600ns voltage-settling time when the AD509 is used as the output amplifier.

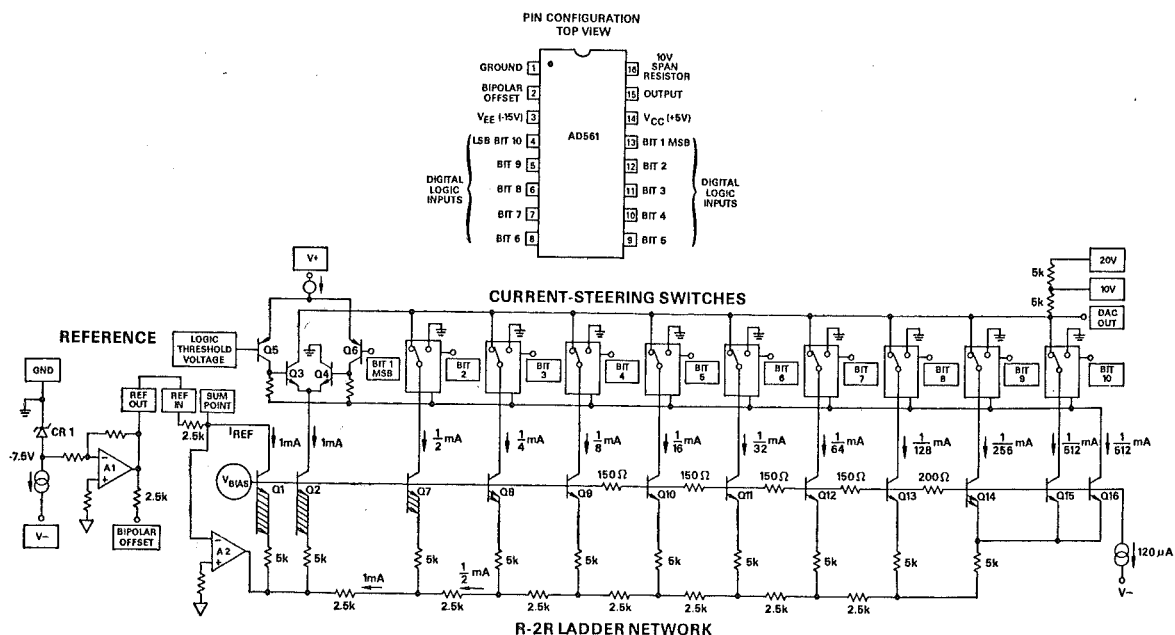


Figure 6. AD561 D/A converter: Schematic and connection diagrams.

● *Integrated Injection Logic conversion – the AD2026 digital panel meter.* I^2L permits analog and high-density logic circuitry to exist as “good neighbors” on a chip manufactured by a bipolar process suitable for high-precision analog circuitry. I^2L eliminates the complexity of conventional bipolar logic by using “inverted” transistors – collectors and emitters are interchanged. When the transistors are inverted, the collectors are isolated without needing the usual wraparound P+ isolation region (which wastes precious “real estate”), and the emitters are grounded.

This leads to very simple logic configurations using interconnection of collectors to provide gating functions.

In the “3.1-digit” AD2026 panel meter (Fig. 7), the I^2L chip contains most of the dual-slope A/D conversion circuitry, including the integrator, comparator, band-gap reference, control logic, clock, counter, display-multiplexer, and display controls. In fact, there are only 13 electrical components in the panel-meter design that are *not* on the chip – 3 light-emitting-diode displays, 3 digit-select transistors, 3 decimal-point current-limiting resistors, 1 LED segment-driver, 2 potentiometers, and the integrating capacitor.

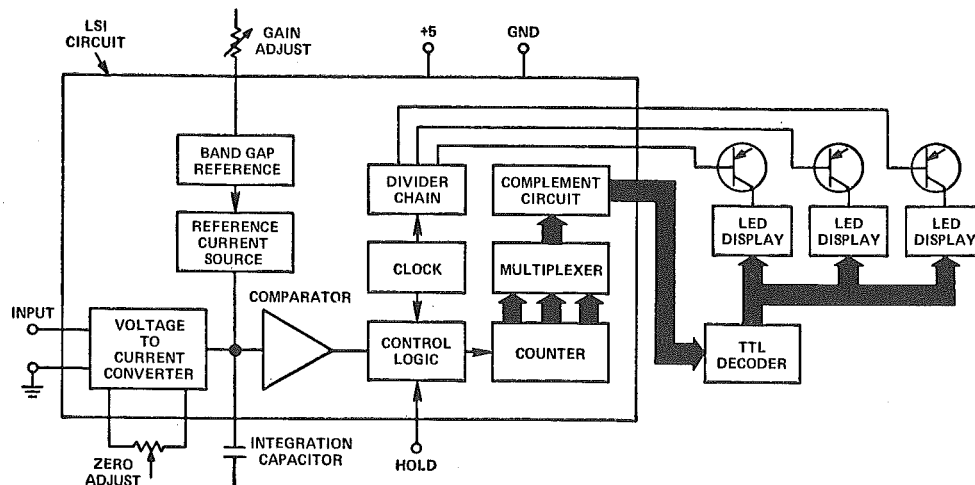


Figure 7. AD2026 block diagram.

I^2L is, in short, a rather promising technique for building monolithic A/D and D/A converters. At this writing, a monolithic 12-bit D/A converter and a monolithic 10-bit A/D converter are close to introduction as new products. They will employ a large part of the arsenal of proven Analog Devices bipolar IC technology, to wit, laser-wafer-trimmed thin-film resistors on an I^2L chip, combining complex logic and high-precision bipolar circuits, and including a buried-Zener reference.

● *Hybrids and Resistance Networks.* As of this writing, completely monolithic 12-bit high-speed (successive-approximations) A/D converters and completely monolithic 12-bit D/A converters with low-impedance voltage (op amp) outputs are not yet manufacturable in quantity with reasonable yields. If we consider the principal advantages of the monolithic technology to be low cost and small size (everything else being more-or-less equal), the next best substitute for monolithic is a dual in-line package (DIP) containing a form of hybrid construction employing a small number of chips on a substrate on which are fabricated both interconnections and resistors. Hybrid technology permits a happy compromise between the functional sophistication of modules and the small size and low cost of IC's.

Until monolithic devices having comparable performance are available, the AD572 A/D converter and the AD564 D/A converter, built with hybrid technology, meet the above requirements for complete 12-bit devices. The AD572 (Figure 8) employs the AD562 basic DAC chips, a reference, buffer-follower (for convenience), comparator, successive-approximations register, and logic circuitry, mounted on a ceramic substrate, which has been fabricated with the resistors and interconnections. The AD564 uses the basic AD562 plus a reference (in the 10V AD2700 class) and an output amplifier.

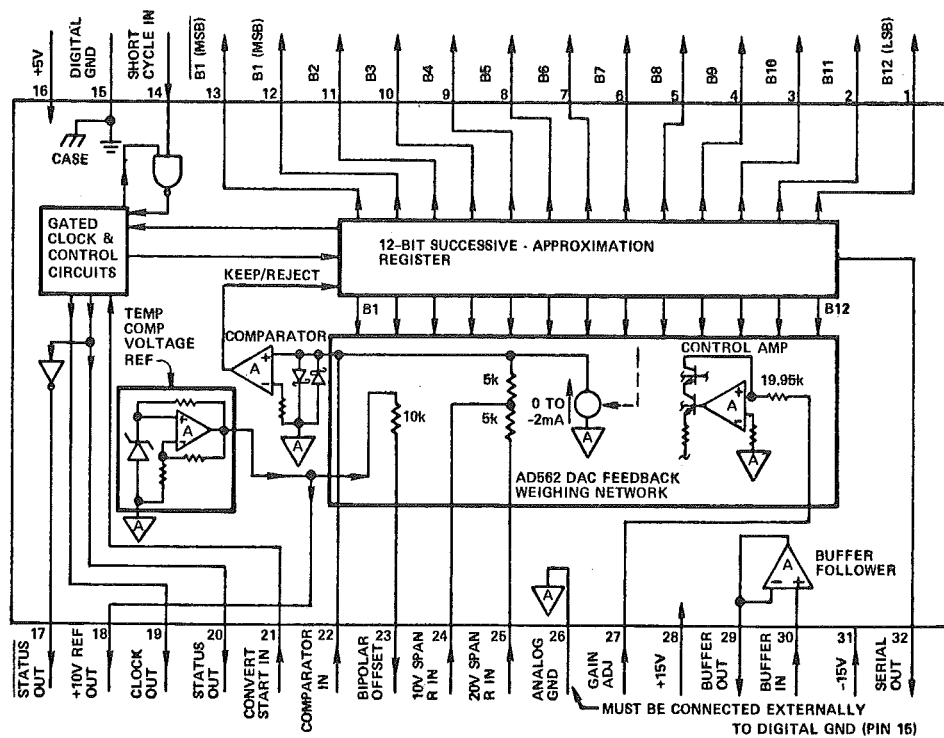


Figure 8. AD572 functional diagram & pinout.

In addition to the buried-Zener technology used in a number of monolithic products that require references, band-gap IC references are also used. The AD580, a 3-terminal reference capable of producing its 2.5V output at currents up to 10mA when operated from 5V logic supplies, is a simple example of the technique (Figure 9). Thin-film-on-silicon resistors help maintain its stability to within 10ppm/°C.

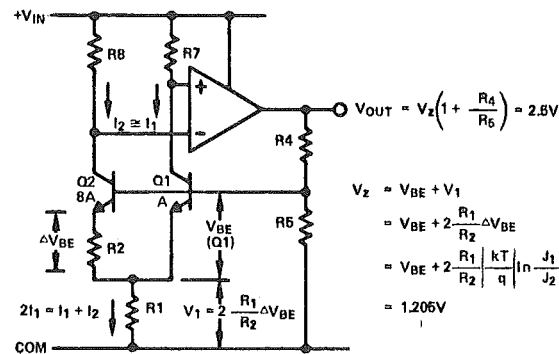


Figure 9. Basic bandgap-reference regulator circuit.

CIRCUIT TECHNIQUES, PERFORMANCE, AND APPLICATIONS

Having discussed the technological variety found in conversion IC's, considered the properties of devices using these technologies, and sated our Readers with generalities, let us now consider some of these devices in greater detail. Our purpose will not be to provide information so complete that the Reader can *design* IC conversion products. Rather, it is to provide: a working knowledge of the relationship between actual circuits and the principles outlined in Chapter II-1, some understanding of the relationship between design and specifications, and a few examples of applications that seem well-suited to each device.

THE AD7520 — A 10-BIT MONOLITHIC CMOS D/A CONVERTER¹

The AD7520 is a 10-bit multiplying digital-to-analog converter constructed on a single silicon chip. It consists of 10 CMOS (complementary metal-oxide semiconductor) switches and

¹ Cecil, J. and Whitmore, J. "A 10-Bit Monolithic CMOS D/A Converter that Can Be Used for 4-Quadrant Multiplication," *Analog Dialogue* 8-1, 1974.

a thin-film-on-CMOS R-2R ladder network. The digital input, which responds to the wide voltage swings of CMOS logic, is also compatible with TTL/DTL logic levels. Two complementary current outputs are available for use with inverting operational amplifiers.

Besides the 10-bit resolution, the AD7520 family has maximum nonlinearities as low as $\pm 0.05\%$ of V_{REF} , nonlinearity temperature-coefficient of $2\text{ppm}/^\circ\text{C}$, and maximum feed-through error of $\frac{1}{2}$ least-significant bit ($\text{LSB} = 0.1\%$) at 100kHz . Typical settling time following a full-scale digital input change is 500ns .

In addition to a constant or variable reference (current or voltage), of either positive or negative polarity, the AD7520 requires one external operational amplifier for unipolar digitally set gains (2-quadrant multiplication) or two amplifiers for bipolar gains (4-quadrant multiplication).

The 74×96 mil ($1.9 \times 2.4\text{mm}$) chip, normally housed in a 16-pin hermetically-sealed ceramic dual in-line package, can also be made available in a flatpack or plastic DIP. It will operate from a single $+5$ or $+15\text{V}$ power supply, and it dissipates only 20mW , including the ladder network.

It can be used for D/A and A/D conversion, multiplication and division, programmable power supplies, digitally programmed filters, and digital-analog function generation. Besides unipolar conversion (of either polarity), offset-binary, two's-complement, and sign-magnitude bipolar operation can also be implemented.

CMOS D/A CONVERSION

Early commercially-available monolithic D/A converters were principally processed by conventional bipolar linear processing techniques. Before 1974, when the AD7520 was introduced, 10-bit conversion had been difficult to obtain with good yields (and low cost) because of the finite β of switching devices, the V_{BE} -matching requirement, the matching and tracking requirements on the diffused-resistance ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

All of these problems were solved or avoided with CMOS devices. They have nearly-infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop; instead, a CMOS switch in the *on* condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature-tracking problems of diffused resistors were solved easily: they weren't used.

The R-2R ladder is composed of $2\text{k}\Omega/\text{square}$ silicon-chromium resistors (a $10\text{k}\Omega$ resistor has a very manageable length/width of 5:1), deposited on the CMOS die. While the absolute temperature coefficient of these resistors is $150\text{ppm}/^\circ\text{C}$, their tracking with temperature is better than $1\text{ppm}/^\circ\text{C}$. The feedback resistor for the output amplifier is also provided on the chip, to ensure that the DAC's gain-temperature coefficient is better than $10\text{ppm}/^\circ\text{C}$ by sidestepping the absolute temperature coefficient of the network.

Finally, the low on-chip dissipation of only 20mW (including the dissipation of the ladder network), in conjunction with the excellent tracking capabilities of the thin-film resistors, minimizes linearity-drift problems caused by internally-generated thermal gradients. It also helps to minimize the power and cooling requirements for circuitry that the AD7520 is used in.

Figure 10 shows a functional diagram of the D/A converter, which employs an inverted R-2R ladder.² Binary-weighted currents flow continuously in the shunt arms of the network; with 10V applied at the reference input, 0.5mA flows in the first, 0.25mA in the second, 0.125mA in the third, and so on. The I_{OUT1} and I_{OUT2} output busses are maintained at ground potential, either by operational-amplifier feedback, or by a direct connection to common.

The switches steer the current to the appropriate output lines in response to the individually-applied logic levels. For example, a "high" digital input to SW1 will cause the 0.5mA of the most-significant bit (MSB) to flow through I_{OUT1} . When the digital input is "low," the

²The inverted R-2R ladder is one of the structures shown in Chapter II-1 (Figure 18).

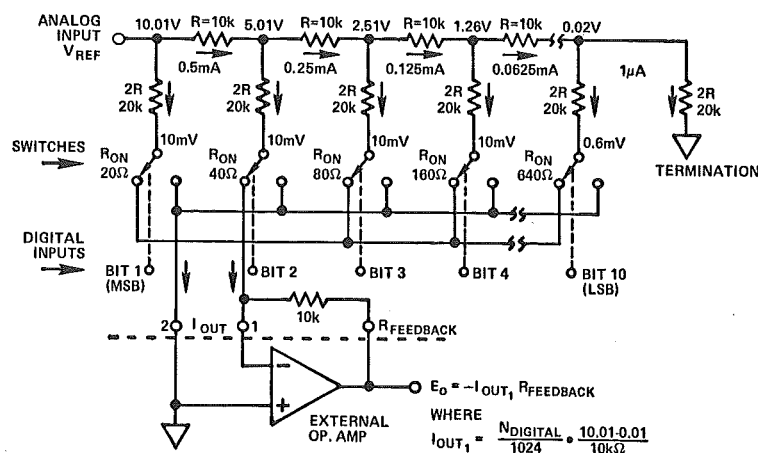


Figure 10. Functional diagram of the AD7520 d/a converter, with $V_{REF} = 10.01V$. Bits 5-9 are omitted for clarity.

current will flow through I_{OUT2} . If I_{OUT1} flows through the summing point of an operational amplifier and I_{OUT2} flows to ground, then "high" logic will cause the nominal output voltage of the op amp to be $-(0.5mA) \times (10k\Omega) = -5V$, for a positive reference voltage of 10V, while "low" logic will make the contribution of Bit 1 zero. With all bits *on* (i.e., "high"), the nominal output will be $-9.99V$. With all bits *off*, the output will be zero.

Linearity errors, and — more important — their variation with temperature, are affected by variations of resistance in both the resistors and the switches. As we have seen, the resistor-network tracking is excellent. However, it is natural to expect that the switches, while tracking one another, will not track the resistance network. With identical switches having realistic resistance values (say 100Ω), one would expect that, as temperature changed, the variation of resistance in the series legs would transform the network into an R - nR network, with n sufficiently different from 2 to destroy the binary character of the network and cause the converter to become non-monotonic.

The key to the linearity of the AD7520 is that the geometries of the switches are tapered so as to obtain *on* resistances that are related in binary fashion, for the first 6 bits. Thus, the nominal values of switch resistance range from 20Ω for the first bit, 40Ω for the second bit, through 640Ω for the last 5 bits. The effect is, as can be seen in Figure 10, to provide equal voltages at the ends of the 6 most-significant arms of the ladder ($0.5mA \times 20\Omega = 0.25mA \times 40\Omega$, etc. = $10mV$). Since this drop is, in effect, in series with the reference, it causes an initial 0.1% scale-factor ("gain") error, which is well within the specifications but does not affect the linearity. Since the switches tend to track one another with temperature, linearity is essentially unaffected by temperature changes, and the gain error is held to within the $10ppm/^{\circ}C$ specification.

Ten-bit linearity could, of course, have been obtained by scaling the *on* resistance of all the switches to a negligible value, say 10Ω , but the switches would have required very large geometries, which would result in a 30% to 50% larger chip, at a substantial increase in cost.

Figure 11 illustrates one of the 10 current switches and its associated internal drive circuitry. The geometries of the input devices 1 & 2 are scaled to provide a switching threshold of

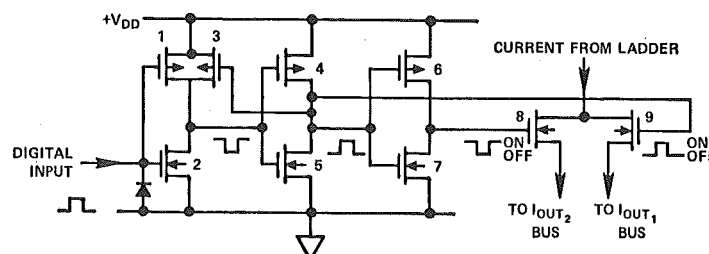


Figure 11. CMOS switch used in the AD7520. Digital input levels may be DTL, TTL, or CMOS.

1.4V, which permits the digital inputs to be compatible with TTL, DTL, and CMOS. The input stage drives two inverters (4, 5, 6, & 7), which in turn drive the N-channel output switches.

EQUIVALENT CIRCUIT

Figure 12 shows the equivalent circuit of the AD7520 at the two extremes of input, all inputs "high" (a) and all inputs "low" (b). V_{REF} (or I_{REF} , if a current reference is used) sees a nominal $10k\Omega$ resistance, regardless of the switch states. The current source $I_{REF}/1024$, represents a 1 LSB current loss through the $20k\Omega$ ladder-termination resistor, shown in Figure 1. R_{ON} , in this case, is the equivalent resistance of all ten switches connected to the I_{OUT1} bus (a) or the I_{OUT2} bus (b). Current-source I_{LKG} , represents junction- and surface-leakage to the substrate. Capacitors C_{OUT1} and C_{OUT2} are the output capacitance-to-ground for the *on* and *off* switches. C_{SD} is the open-switch capacitance.

The 1000:1 ratio between R_{ladder} and R_{ON} provides a number of benefits, all related to the small voltage drop across R_{ON} :

- V_{REF} can assume values exceeding the absolute-maximum CMOS rating, V_{DD} . For example, V_{REF} could be as large as $\pm 25V$, even if the AD7520's V_{DD} rating were only $+17V$.
- The nonlinearity temperature-coefficient depends primarily on how well the ladder resistances track. Since R_{ON} is only a small fraction of R_{ladder} , any R_{ON} tracking errors will be felt only as 2nd- and 3rd-order effects.
- The same argument holds true for power-supply variations. Any change of switch *on* resistance, as the power supply changes, will be swamped by the 1000:1 attenuation factor. Power-supply rejection is better than 1/3 LSB per volt.
- If V_{REF} is a fast ac signal, the feedthrough coupling via C_{SD} , the open-switch capacitance, will be negligible, again because of the 1000:1 voltage stepdown. The parasitic capacitances from V_{REF} to I_{OUT1} and I_{OUT2} comprise the major source of ac feedthrough. Careful board layout by the user can result in less than $\frac{1}{2}$ LSB of ac feedthrough at 100kHz.

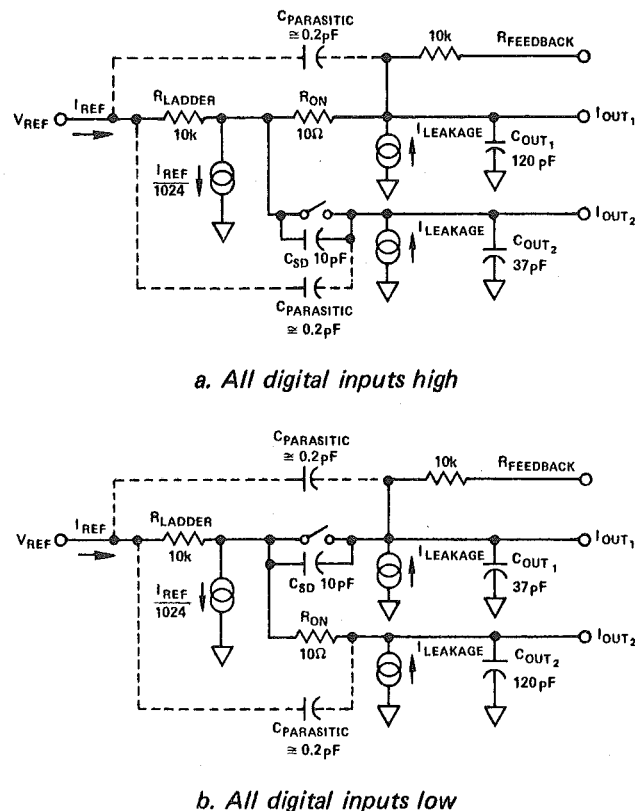


Figure 12. Equivalent circuits of the AD7520 D/A converter.

Since the *on* resistance depends only on the value of V_{DD} , not the current through the switch, and the resistance network is unaffected by V_{REF} , the full-scale output current (all bits "high") is nominally $V_{REF}/10.01k\Omega$, less the "constant" current losses shown in Figure 12. This means that I_{OUT} is almost perfectly proportional to V_{REF} over the whole range from -10V to +10V. Equally important, the conversion linearity error (0.05%) is independent of the sign or magnitude of V_{REF} .

The extremely low analog-linearity error at constant digital input results in excellent fidelity to the input waveform, which suggests some interesting possibilities for the AD7520 in the calibration and control of gain in signal generators, high-fidelity amplifiers, and response-testing systems.

APPLYING THE AD7520

The two most common forms of application are in unipolar D/A conversion (2-quadrant multiplication) and bipolar offset-binary conversion (4-quadrant multiplication), shown in Figures 13 and 14. Where high speed is not desired, the output amplifier may be an AD741. For faster response, the AD518, AD505, or AD509 may be used, with appropriate compensation and a 10-20pF feedback capacitor.

Unipolar conversion. The response equation for Figure 13 is nominally

$$E_O = - \frac{N_{\text{binary}}}{1024} V_{REF} \quad (1)$$

Responses to typical codes are tabulated. Since V_{REF} may be positive or negative, two-quadrant multiplication is inherent. Circuit gain is easily trimmed by adjusting V_{REF} , inserting adjustable resistance in series with V_{REF} or R_{feedback} , or by tweaking scale factors elsewhere in the system. As noted elsewhere, once set, using low-TC trim resistors, gain stability with temperature is excellent.

Unlike truly passive potentiometers, CMOS devices, like the AD7520 (and the AD7522 and AD7570, to be discussed further on) *must* have their analog outputs at ground level to maintain conversion linearity in the forward direction and to protect the switches in the reverse direction (in other words, their output voltage compliance is negligible). Therefore, their outputs should be connected to op-amp summing points for all applications save for nulling (e.g., with comparators in A/D converters). In any event, it is a sensible practice to *always* use a Schottky diode, connected between the current output and ground, as shown in Figure 13, even if — for the sake of clarity — it is omitted from an application sketch.

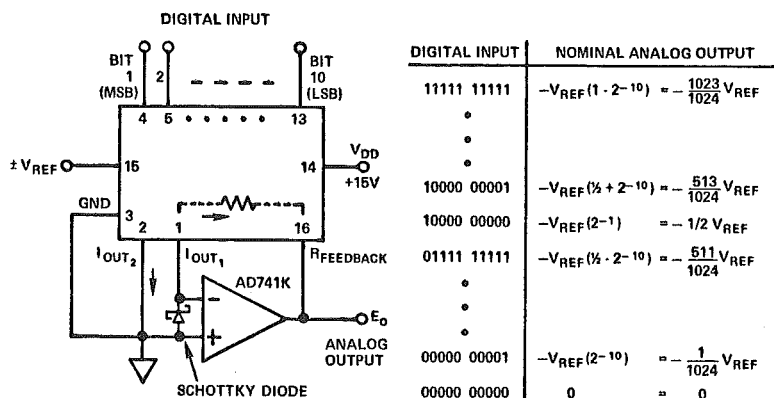


Figure 13. The AD7520 as a unipolar binary digital to voltage converter (2-quadrant multiplier).

Bipolar conversion. The offset binary response equation for Figure 14 is nominally

$$E_O = - \left[\frac{N_{\text{binary}}}{512} - 1 \right] V_{REF}$$

Responses to typical codes are tabulated. If the MSB is complemented, the conversion relationship will be recognized as appropriate for a 2's-complement input, but with a negative scale factor. The MSB determines the sign, and the last 9 bits determine the magnitude in 2's complement notation. Since V_{REF} may be positive or negative, 4-quadrant multiplication is inherent.

In this configuration, I_{OUT2} , which is the complement of I_{OUT1} , is inverted and added to I_{OUT1} , halving the resolution (of each polarity) and doubling the gain. The $10M\Omega$ resistor corrects for a $1/1024$ difference (inherent in this technique) between I_{OUT1} and I_{OUT2} at zero (10000 00000). A2 is shown as a current inverter, but it might also be a voltage inverter, if the AD505 is used.

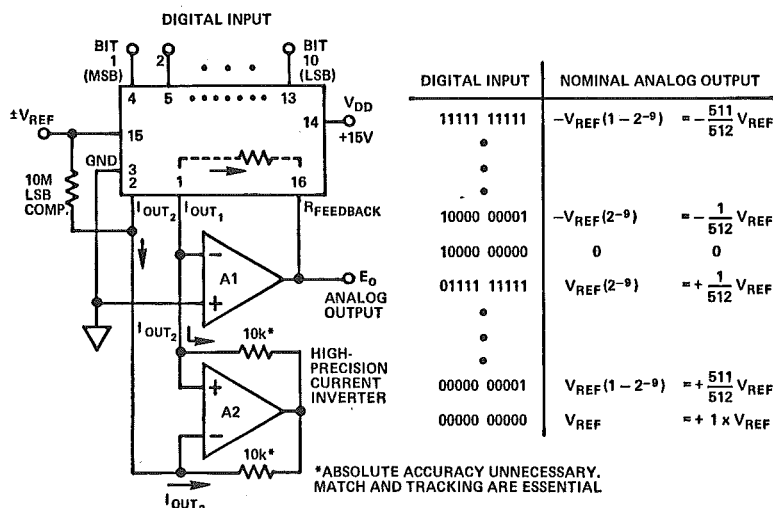


Figure 14. The AD7520 as a bipolar offset-binary digital-to-voltage converter (4-quadrant multiplier).

If sign-magnitude coding is desired, to obtain bipolar conversion with the full 10-bit-plus sign resolution, the output of the *unipolar conversion* circuit may be fed into a sign-magnitude converter, such as Figure 15. An AD7510 DI quad switch will handle two such circuits.

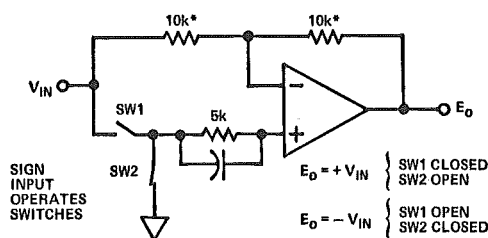


Figure 15. Sign-magnitude to bipolar converter.

ANALOG DIVISION

Since one form of analog division circuit is a multiplier in a feedback loop, one might consider the divider circuit² shown in Figure 16. In this circuit, the feedback current from the converter's "reference" input to the summing point of the op amp is proportional to (i.e., multiplied by) the digital number; but it must also be equal to the current developed through the input resistor. Therefore the op-amp output is constrained to depend on the ratio of the input signal to the gain value of the digital number. Note that the AD7520 in such an application is inherently a 2-quadrant divider, since the input signal (and the inverted output) can be either positive or negative. Connected as shown, the gain magnitude varies from a minimum of $1024/1023$ to (theoretically) $1024/0$, the open-loop gain of the op amp; the largest controlled gain is $1024/1$. At the higher gains, accuracy is lost because the feedback

² Whitmore, J. "Ways of Using the AD7520," *Analog Dialogue* 8-2, 1974.

attenuation for small numbers may only be accurate to within $\frac{1}{2}$ LSB; for example, at a gain of 1024, if the LSB has an error of 10%, the gain will be in error by that amount. Naturally, accuracy rapidly improves with increasing denominator magnitude, and the error will typically be less than 0.05% at full-scale denominator, after adjustment.

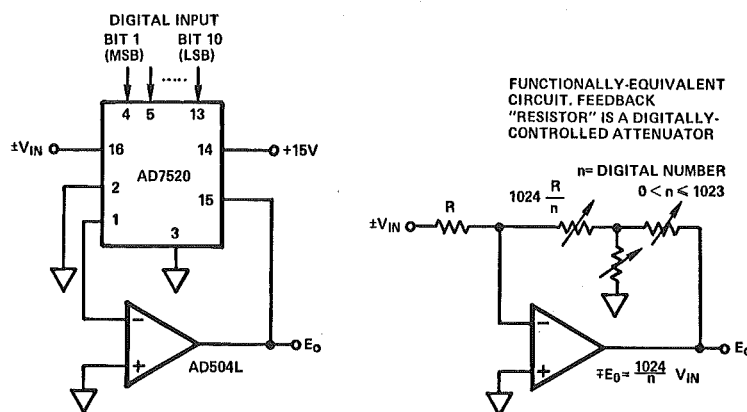


Figure 16. An analog-digital divider.

SINGLE-SUPPLY APPLICATION

In computerized process-control systems,³ digital-to-analog converters are typically used to manipulate set-points and operate valves. General-purpose DAC's, such as the AD7520, usually involve inverting op amps, which call for dual power supplies. However, one-sided supplies are highly desirable because of their lower cost, better reliability, and their compatibility with the 4–20mA range used in transmission of electrical control signals in process-control systems.

The single-supply scheme of Figure 17 employs the AD7520, with an LM324 single-supply quad op amp, and an AD2700 precision 10V reference, to provide a jumper-selected choice of two output voltage ranges, 0–10V and 2–10V. The latter range can be directly transduced into 4–20mA and 10–50mA current ranges appropriate for control systems, by schemes such as that shown.

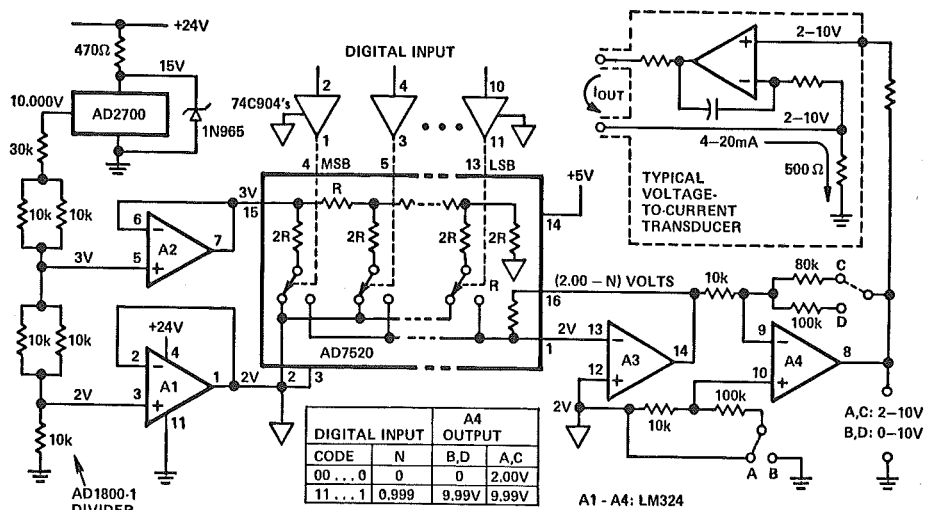


Figure 17. Single-supply 10-bit DAC circuit.

In the circuit of Figure 17, the +24V supply is tapped at +5V for TTL logic levels. The AD2700 reference develops a precise 10 volts without needing adjustment. It is stepped down to +3V and +2V, which appear at the outputs of followers A2 and A1. The 2V output of A1 becomes the reference-ground level for the AD7520 DAC, the inverting op amp, A3, and the two 74C904 Hex Non-Inverting Buffers, which drive the logic inputs of the AD7520 (10 of the 12 buffer channels are used).

³Clark, V.R., "D/A Conversion with a Single-Supply Circuit," *Analog Dialogue* 10-1, 1976.

The net 1V reference voltage applied to the DAC is scaled in proportion to the digital input number (N) and inverted by amplifier A3 at unity gain. The output of A3 swings from 2V to 1.001V as N varies from 0 to $1 - 2^{-10}$. Depending on the jumper connections, the 0-to-full-scale output swing of A4 is either 0–10V or 2–10V. The 2–10V range ($E_4 = 2 + 8N$ volts) can directly scale a current-transducer output, such as the one shown, for 4–20mA or 10–50mA. The actual system uses a proprietary design, capable of generating a grounded or floating source or sink current.

AUDIO-CIRCUIT APPLICATIONS.⁴

High-resolution, high-linearity multiplying DAC's that handle both polarities of analog input become quite attractive to the designer of audio signal-processing equipment when these benefits are combined with wide bandwidth and low cost.

Monolithic IC DAC's available before the advent of the AD7520 generally had less resolution and a limited range of reference variation. The lack of both reference-voltage source and output amplifier is not an important limitation in audio use. In fact, the number-one advantage is that the reference-input voltage swing can exceed $\pm 10V$, with excellent linearity and bandwidth. Although one would expect a "multiplying DAC" to have this capability, not all types possess it fully.

AD7520's can be used with bipolar voltages from volts down to millivolts. Correct and linear ratiometric operation under such conditions makes them ideal scaling elements for audio signals. Since they can be viewed as digitally-programmable attenuators, they can marry high-quality and audio signal-processing circuits to digitally based systems under microprocessor control.

Besides the classical DAC specs of conversion linearity, resolution, etc., the special considerations for audio use include distortion, noise, and crosstalk in the "off" state.

Typical measurements of distortion are of the order of 0.05% or less over the audio band. This is due to the linearity enforced by the thin-film R-2R ladder, which ensures a linear summing-point current in the presence of a varying reference (input) voltage at a given digitally set gain.

Noise is a parameter that can be determined from the data sheet; it is determined by the thin-film network's nominally $10k\Omega$ characteristic resistance. This contrasts favorably with some active types of DAC's, which are noisier.

Reference-input feedthrough is specified on the data sheet as 10mV p-p (max) for 20V p-p input at 100kHz (-66dB). This, being but one point on a curve, doesn't tell the whole story. At lower frequencies, feedthrough is much less, with a floor of $\leq -90dB$ at 1kHz (Figure 18). Feedthrough is essentially capacitively coupled crosstalk. It is layout-sensitive.

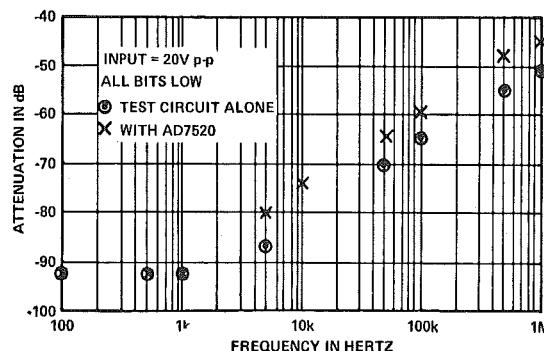


Figure 18. AD7520 feedthrough measurement.

Control-signal feedthrough is undesirable in audio gain control, since it can cause thumps, pops, or clicks. Because there is no bias current in the AD7520/21/22, the output contains the desired signal current only, avoiding dc level shifts. The narrow switching spikes can be filtered without loss of bandwidth.

⁴ Jung, W. "Audio Applications Ideas for CMOS DAC's," *Analog Dialogue* 10-1, 1976

It is interesting to consider the AD7520/21/22 accuracy in relation to the needs of audio level control. Without trim, the full-scale gain error is typically 0.3%, or, in conventional audio parlance, $\pm 0.026\text{dB}$. Even adding the loosest (conversion) nonlinearity† error, the gain error is still only $\pm 0.043\text{dB}$, adequate for a great number of audio applications, without trimming or tweaking. Remember that 1dB is close to the threshold of human perception of gain changes.

For applications where it is desirable to trim the DAC gain exactly to unity, given the possibility that it may be either high or low, resistance may be added in series with either the input (V_{REF}) terminal or the feedback terminal. Figure 19 shows a way of dealing with either contingency with one pot.

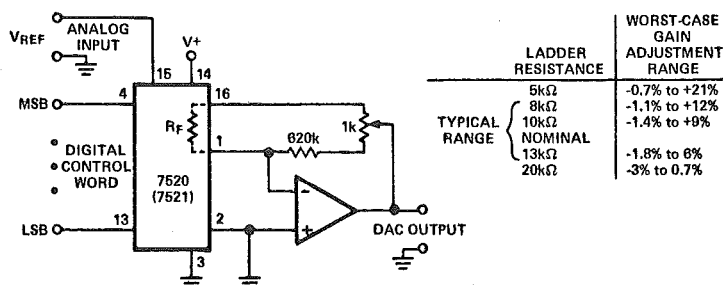


Figure 19. Single-control trim for gain calibration, allowing for a large range of absolute ladder-resistance variation.

Figure 20 shows a basic circuit using the AD7520 as an audio gain control. A low-cost AD301A, used as the output buffer, is operated in the feedforward mode, for a gain-bandwidth of 30MHz and a $10\text{V}/\mu\text{s}$ slewing rate. This combination, using the lowest-cost “J”-suffix DAC, provides perhaps the most cost-effective, high-performance combination for an audio gain-control of this class. It can of course also be used as a general-purpose DAC, with device choice tailored to desired performance. Settling time to $\frac{1}{2}\text{LSB}$ (10 bits) is $6\mu\text{s}$.

In general, the application of high-speed-DAC circuits to audio use can give rise to some serious problems. For instance, if the channel gain is to be manipulated while signals are present, large instantaneous gain changes in the presence of signal peaks will almost guarantee annoying audible switching-transients due to the abrupt change in level.

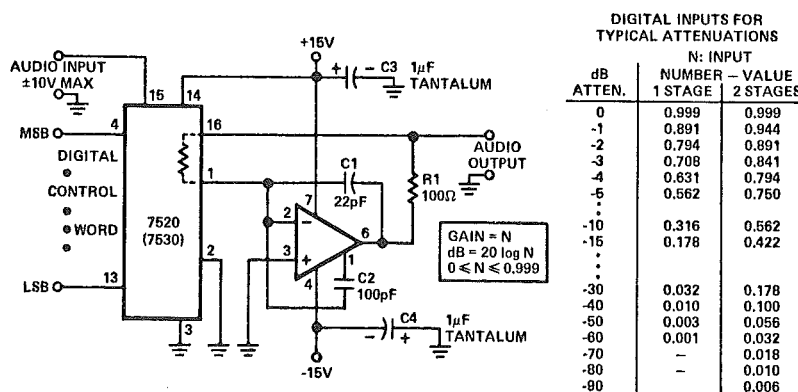


Figure 20. Inexpensive, high-performance gain control.

As a remedy, one might restrict gain-switching to times when the signal is near zero. A more pleasing and satisfactory approach is to spread the gain change over about 50ms or more by digitally “ramping” it, using a clock and preset counter. If sufficient resolution exists, the staircase effect should be imperceptible. With an 8-bit converter, this permits 48dB of staircasing. Avoid slew-limiting in the DAC output amplifier; it can cause noxious distortion for sufficiently large gain steps, another reason for using controlled-gain steps and fast amplifiers.

†Conversion-linearity errors affect only gain, not analog linearity.

Additional gain range can be obtained by cascading decade blocks of gain, or by cascading DAC's, with common digital input. If you wish to obtain the natural benefits of equal-dB gain steps, the digital number applied to the DAC(s) should vary exponentially. For m cascaded DAC's with $-k$ dB of attenuation, the value, N , of the common digital input should be

$$N = (10)^{k/(20m)} \quad (1)$$

This can be achieved via software instructions in a computer system; it can also be achieved by means of programmable read-only memory (PROM), between the counter output and the DAC(s). Note that only about 2 significant digits are needed for accuracy to within 1dB, from the examples in the table (Figure 20).

Figure 21 illustrates in principle a variation of the basic gain controller which can be used to steer or "pan" an audio signal between two output channels, another common audio processing requirement. The two gains are simply made complementary. Thus, the signal will be fully *left* for all 1's, full-*right* for all 0's, and deployed equally for just the MSB on.

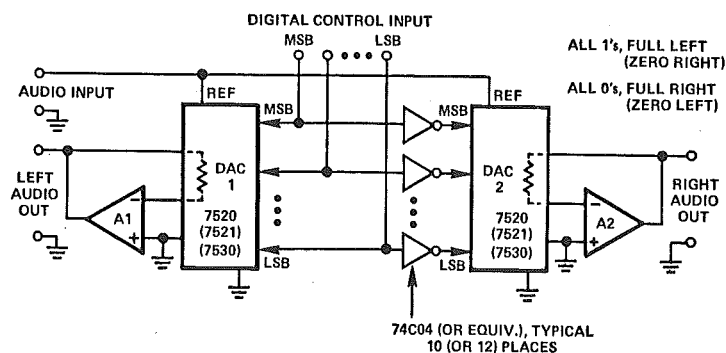


Figure 21. Digitally-programmed audio panner.

In a simpler version (Figure 22) a single DAC is used. Here, the I_{OUT2} line of a 7520, normally grounded, is used to drive a second summing amplifier with an external feedback resistor, R_{f2} . Since the current at I_{OUT2} is inherently the complement of I_{OUT1} , the circuit will work as a complementary panner. The drawback is the necessity to trim R_{f2} for equal channel gains (MSB on); since the external resistor will in general not track the network, the panner may not retain its accuracy for wide temperature variations. However, the method is simple and attractive for non-critical applications.

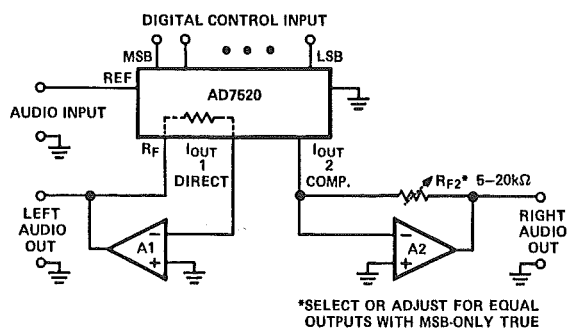


Figure 22. Simplified audio panner.

DAC's are useful for generating, as well as controlling, signals. Figure 23 shows a simple scheme for digitally programming the output frequency of a standard integrator-comparator function generator^{5,6}. The timing resistor (the input resistor to the integrator) is replaced by the DAC's R-2R ladder. Since frequency is proportional to the integrator input current, it will be proportional to the digital input to the DAC.

A calibration control with wide latitude is needed because of the loose tolerance on absolute value of the R-2R ladder resistance; also, as noted above, tracking errors with temperature

⁵ *Nonlinear Circuits Handbook*, Analog Devices, Inc., 502pp., \$5.95 (soft).

⁶ *Audio IC Op-Amp Applications*, W.G. Jung, Howard W. Sams & Co., Inc. Indianapolis, Indiana 46206 (soft).

will limit stability. Fast amplifiers, such as the AD301A (with feedforward in the integrator) are cost-effective.

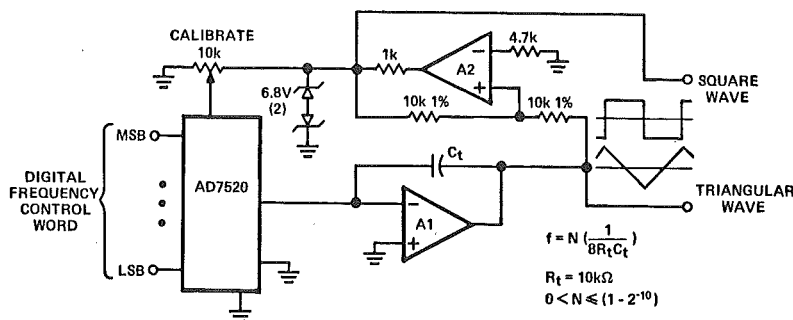


Figure 23. Programmable function generator; *p-p* amplitude of both waveforms is $\cong 15V$.

There are myriad uses for these versatile DAC's; many have been documented here in the past, and more are sure to come. In audio alone, programmable oscillators, equalizers, filters, etc., may provide the Reader with food for thought.

A final word. Here are some suggestions for getting best results with the AD7520 and similar CMOS DAC's:

1. Tie unused CMOS digital inputs either high or low; don't leave them open.
2. Remember that the current-summing junction is loaded by a capacitance from 40pF to 120pF. If fast amplifiers are used, phase compensation is required for stability (e.g., the usual shunt feedback capacitance across $R_{FEEDBACK}$).
3. The amplifier offset should be minimized to maintain device linearity.
4. The I_{OUT1} and I_{OUT2} terminals should never be allowed to go negative by 1 V_{BE} drop — a Schottky diode to ground, as in Figure 13, is recommended.

THE AD7522 — A DOUBLE-BUFFERED 10-BIT CMOS MULTIPLYING DAC⁷

The AD7522 is a systems-compatible 10-bit multiplying D/A converter, fabricated on a single 3 x 2.2mm (118 x 89 mil) silicon die, and packaged in a 28-pin plastic or ceramic dual in-line package. Like the AD7520, it has 10 SPDT N-channel current-steering switches and a thin-film-on-CMOS R-2R ladder attenuator for current weighting. *In addition*, it has a dual-rank input storage system consisting of 10 "D"-type level-triggered holding latches and a 10-bit edge-triggered serial/parallel input-loading register (which in turn consists of 2 controllable "bytes", of 8- and 2-bit capacity), as was shown in Figure 2 of this chapter.

Basic unipolar operation (either fixed-reference or 2-quadrant multiplication) requires only the addition of an external positive-or-negative, constant-or-variable, "reference" voltage or current and an operational amplifier (Figure 24). For bipolar conversion (4-quadrant multiplication), with offset-binary or 2's complement coding, one additional operational amplifier is needed (see Figure 14).

The main (V_{DD}) supply requires a nominal +15V @ 2mA *max*; 1μA is typical, since most of the current is required only during switching. The choice of the logic (V_{CC}) supply depends on the logic-interface requirements. For example, if $V_{CC} = +5V$, the digital inputs are TTL-compatible. If $V_{CC} = +10V$ to +15V, the digital inputs-and-outputs are CMOS compatible.

Three grades of conversion linearity are offered — 8, 9, and 10 bits. Typical current-settling time following a full-scale code change on the digital inputs is 500ns.

The most-interesting aspect of the AD7522 to the system designer is the DAC's double-buffered input structure, offering tremendous versatility, yet still seldom found, even in

⁷Whitmore, J. "Monolithic 10-Bit CMOS Multiplying DAC Provides Direct Interface to Data-Bus Inputs," *Analog Dialogue* 9-3, 1975.

discrete-module D/A converters. Salient features include:

1. Logic-controlled choice of serial or parallel loading.
2. A "load/display" choice, which either allows new data to update the DAC, or locks out unwanted data appearing at the digital inputs. If the AD7522 is used with a CPU data bus, this "lockout" function allows the CPU or other I/O peripheral to place data on the bus without altering data that was previously loaded into the AD7522.
3. Byte-serial (or parallel) loading allows a 10-bit word to be loaded into the DAC from either an 8-bit micro-computer data bus, or from a 10-or-more-bit paralleled line.
4. A serial *output* allows recovery of data from the input register.
5. A short-cycle feature allows 8 bits, to the MSB, to be loaded serially.

A summary of the AD7522 functions, and where to find them in Figure 2, is given in a box on the next page.

The advantages of ADI's thin-film-on-CMOS process, again briefly summarized, are:

- High logic density and low dissipation (hence good yields and low cost).
- No β and V_{BE} problems.
- Since switches are bidirectional, both polarities of analog signals are inherent.
- SiCr resistor networks have better linearity and tracking than diffused resistors.

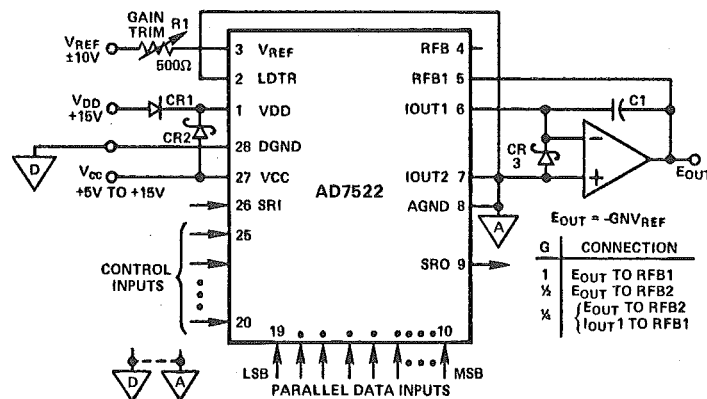


Figure 24. Connecting the AD7522 for unipolar D/A conversion. N is a fractional 10-bit binary number from 0 to $(1 - 2^{-10})$.

APPLICATIONS

The AD7522 can perform all of the conversion functions that are performed by the AD7520, but with the added flexibility of communication with digital systems. However, as a second-generation DAC, it has a few improvements that facilitate analog applications as well. First of all, there are separate analog and digital ground returns. Figure 24 shows how the AD7522 is connected for a unipolar conversion relationship. The feedback resistor is center-tapped, which allows a choice of full-scale gain of 1, $\frac{1}{2}$, or $\frac{1}{4}$. The termination of the ladder, instead of being grounded internally, is brought out to a terminal; this permits bipolar (4-quadrant multiplier) circuits to be instrumented with fewer external resistors than is the case with AD7520.

Two, among many, of the digital-communication possibilities are shown in Figures 25 and 26. Figure 25 illustrates serial operation, and Figure 26 shows how the AD7522 might be connected to a microprocessor bus for byte-serial updating.

It is easy to see that it is a simple matter for a microprocessor to first load the 8 least-significant bits into the 8-bit register, then load the two most-significant bits into the 2-bit register, and finally, to strobe 10-bit data into the output register, for the D/A converter. Note that the DAC register can also accept data in the form of a stream of 10 serial bits — and shift them out as well as in.

(Refer to Figure 2)

FUNCTION	PIN NO.	MNEMONIC NOTATION
DIGITAL – Data (positive-true with respect to I_{OUT1})		
Parallel Data Input, Data-Bit 9 (MSB) to Data-Bit 0 (LSB) ⁸	10–19	DB9 through DB0 ⁸
SeRial Input	26	SRI
SeRial Output (NRZ) – Auxiliary output for recovering data stored in the input register	9	SRO
DIGITAL – Control		
Serial/Parallel Control – If “0”, parallel data will be loaded into input registers DB0-DB9 when LBS and HBS are exercised; if “1”, serial data will be shifted through input registers when clocked in with LBS and HBS.	21	SPC
High-Byte Strobe – In the <i>parallel</i> mode, positive edge strobes parallel data appearing on DB8 and DB9 into the input register; in <i>serial</i> , positive edges advance data through the input shift register.	25	HBS
Low-Byte Strobe – Same functions as HBS, for DB0 through DB7	24	LBS
Load/Display DAC Strobe – If “0”, AD7522 is in “display” mode, digital activity in input register is locked out; if “1”, data in the input register is strobed into the DAC.	22	LDAC
Short-Cycle (8 bits) – In <i>serial</i> , if “0”, 2 LSB's are bypassed for proper loading of 8 bits; if “1”, a full 10-bit serial word is accepted.	20	$\overline{SC8}$
ANALOG		
Reference Input – Constant or variable ac or dc voltage in the $\pm 25V$ range is proportionally scaled (gain-adjusted) by the input digital word.	3	V_{REF}
Output Current – Normally connected to summing point of the output op amp; bit-currents flow for “1” DB's.	6	IOUT1
Complementary Output – Normally grounded (unipolar) or connected to summing point of inverting op amp (bipolar); bit currents flow for “0” DB's.	7	IOUT2
Feedback Resistor (F.S. Gain = 1) One end is connected internally to I_{OUT1} . RFB1 is connected to op-amp output for normal unity-gain operation, or to summing point for gain of $\frac{1}{4}$; no connection for gain of $\frac{1}{2}$.	5	RFB1
Feedback Resistor Center-Tap (F.S. Gain = $\frac{1}{2}$)—Connected to op-amp output for gain of $\frac{1}{2}$ or $\frac{1}{4}$.	4	RFB2
Ladder Termination – Grounded for unipolar gain; connected to I_{OUT2} for bipolar gain.	2	LDTR
SERVICE		
Main Supply – +15V nominal	1	V_{DD}
Logic Supply – +5V for TTL compatibility; +10V to +15V for CMOS compatibility	27	V_{CC}
Digital Ground	28	DGND
Analog Ground – Back gate of the DAC's N-channel single-pole, double-throw (SPDT) current-steering switches.	8	AGND

⁸ See the discussion, “A Note on Bit-Labeling,” near Figure 12 of Chapter I-4.

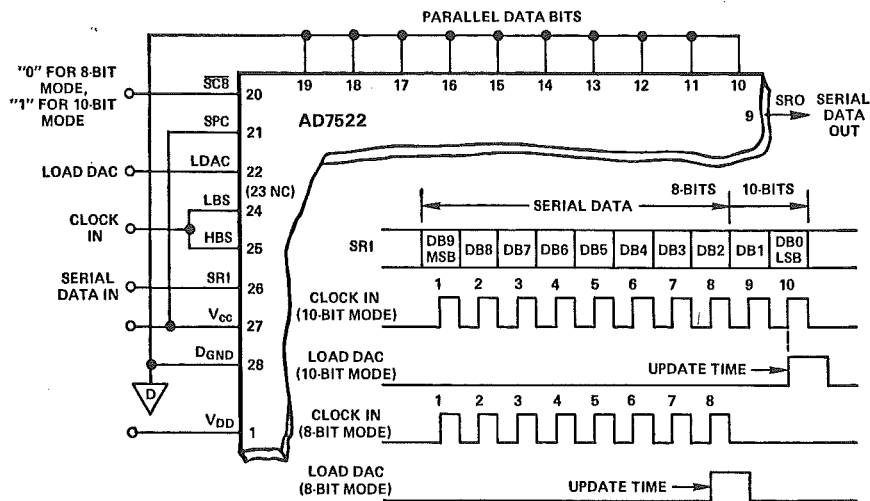


Figure 25. Serial 8- and 10-bit loading. Analog connections omitted for clarity.

Figure 26 shows how the AD7522 is connected into an 8-bit data bus. The bus is wired directly to the 8 least-significant bits; and the two most-significant bits of the converter are wired to the two least-significant bits of the bus.⁸

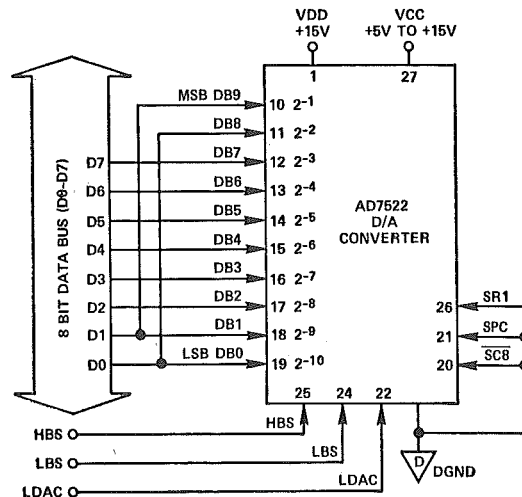


Figure 26. AD7522 - Connection for 2 byte operation.

Figure 27 shows two AD7522's (configured as in Figure 26), interfaced to an "ideal" microprocessor as memory. Since the AD7522 was designed as a compromise for both parallel and byte-serial operation, the external address-decoding logic is necessary as shown. Nevertheless, the interface is extremely simple and can allow either simultaneous or non-simultaneous update of the two D/A converters. The *or* gates allow a single memory address to update the output registers of both D/A converters simultaneously. It is worth noting that many μ P's (the 8080 included) incorporate 16-bit data instructions, which would allow the processor to output the data to both converters with a single *memory-write* instruction.

THE AD7570 - A 10-BIT SUCCESSIVE-APPROXIMATIONS CMOS A/D CONVERTER⁹

The AD7570 is a 10-bit Analog-to-Digital converter on a single 120 x 135 mil (3 x 3.4mm) chip, packaged in a 28-pin dual in-line hermetically-sealed ceramic enclosure. It consists (Figure 3) of a 10-bit D/A converter and the associated logic circuitry required to perform a conversion using the successive-approximations technique. Its analog inputs can be either

⁸ See the discussion, "A Note on Bit-Labeling," near Figure 12 of Chapter I-4.

⁹ Whitmore, J. and Van Aken, R. "10-Bit Monolithic CMOS A/D Converter," *Analog Dialogue* 9-2, 1975.

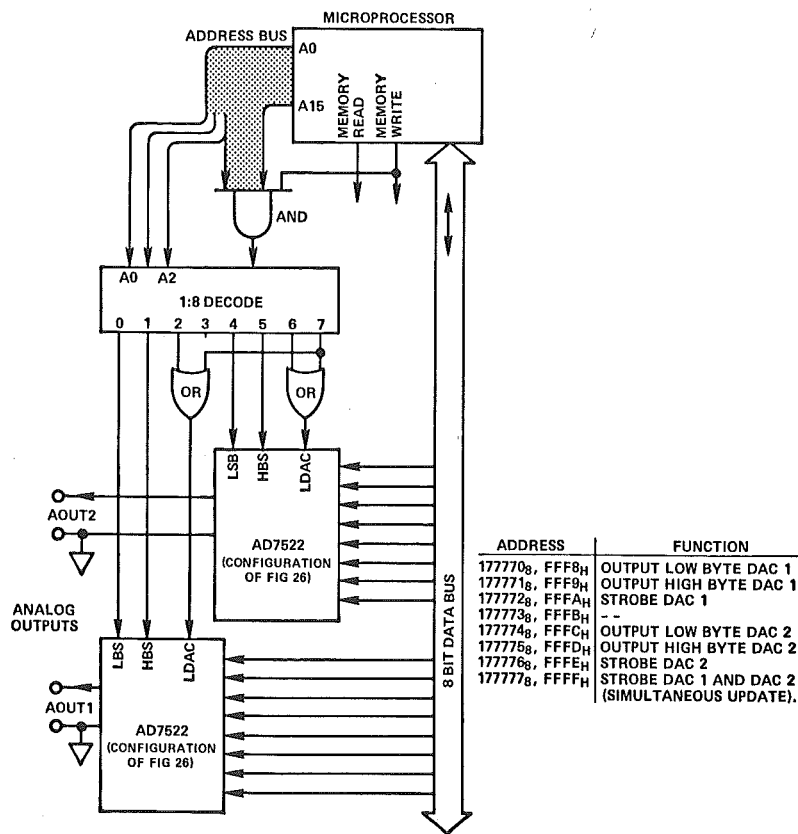
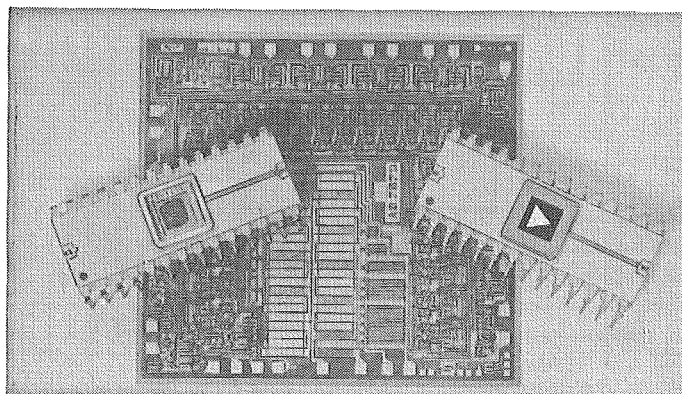


Figure 27. Interfacing multiple AD7522's to a microprocessor.

single-ended (of either polarity) or bipolar using an external inverting op amp. It interfaces with DTL/TTL or CMOS logic and has both serial and parallel outputs, with a number of interesting features designed to make it readily usable in complex data-acquisition systems (for example, with 8-bit microprocessor busses).

Its external operational requirements are 20mW of power (V_{DD} of +15V and V_{CC} of 5 to 15V), an external reference (which allows ratiometric operation and choice of input polarity), an external RC circuit to determine the internal clock frequency, or an external clock (for a wide range of conversion frequencies), and a comparator, such as the AD311 (for best tradeoff between accuracy, conversion-speed, and cost). For bipolar operation, a low-cost external op amp preconditions the analog input.



The AD7570 will accurately digitize signals having full-scale ranges from nearly $\pm 25V$ down to levels limited only by the comparator's ability to detect submillivolt changes. This is a direct consequence of the use of a highly linear on-board multiplying D/A converter (closely related to the AD7520), which can accept a wide range of reference voltage. Normal operation is specified with 10V reference.

Available with 8- or 10-bit linearity (J or L versions, short-cycle-able to 8-bit resolution for increased speed), 40 μ s conversion time (10 bits), and $\pm\frac{1}{2}$ LSB differential nonlinearity (over the temperature range), the AD7570 has a gain-temperature coefficient better than 10ppm/ $^{\circ}$ C.

MICROPROCESSOR CAPABILITY

As noted above, the AD7570 is specifically designed for ease of use in "data-bus" systems, where its three-state outputs are under external control. There are several features of especial interest:

- The parallel data outputs⁸ (bits 0-9) and the conversion status line are "three-state", that is, they are essentially disconnected from the common data bus until appropriate interrogation signals are received. (Data ready? High bits? Low bits?)
- The two most-significant bits and the 8 lower bits can be separately interrogated: this permits all 10 bits to be furnished on an 8-bit common data-bus in two bytes.
- The serial output (non-return-to-zero) and an associated synchronized clock output are also provided with 3-state outputs. The serial output is generated as the conversion proceeds; it and its associated SYNC output float at other times. To interrogate it, in bus applications, a conversion is started.
- The AD7570 can, of course, also be used with fully-committed connections, by connecting the three-state control inputs to the appropriate logic levels for the desired permanent mode of operation.

ADVANTAGES OF CMOS

The most-obvious reason for using CMOS construction is the low power dissipation. For example, an inverter consists of a stack of two complementary devices. When one is *on* (low voltage drop), the other is *off* (low leakage current). Since the output is always very near one or the other power-supply rail (except when switching), little continuous power is dissipated. The total power drain of the AD7570 is 20mW.

The low dissipation allows greater circuit density. Besides this, the CMOS process employed in the AD7570, which involves a two-layer metal-interconnect scheme, allows a 30% further reduction in chip size, to a reasonable, manufacturable 120 x 135 mils (3 x 3.4mm), with good yield.

The most important advantages of CMOS are realized in the D/A converter, which is the critical element in a successive-approximations converter. This topic has been covered in substantial detail in relation to the design of the AD7520, which the AD7570's DAC very

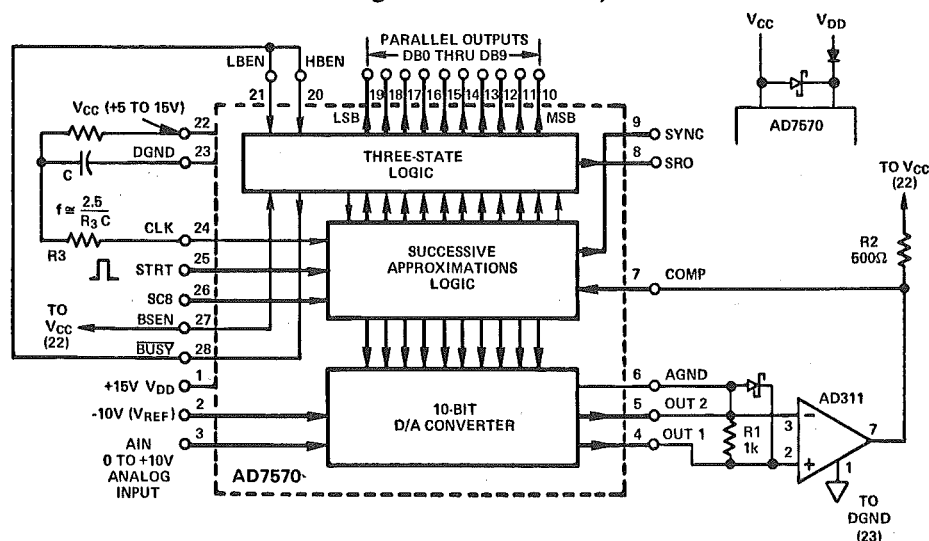


Figure 28. Operational connections for A/D conversion with positive (unipolar) analog input and internal clock. Parallel outputs are enabled when status (BUSY) goes high. The protective diodes indicated should be used in all applications.

⁸See the discussion, "A Note on Bit-Labeling," near Figure 12 of Chapter I-4.

much resembles. Briefly, the deposition of a thin-film high-precision R-2R ladder network on a chip with low-dissipation CMOS switches eliminates problems caused by: finite transistor β and its variations, transistor V_{BE} and its variations, diffused-resistor matching and tracking, and drifts of gain and linearity caused by thermal gradients on the chip (as a result of sizeable dissipations). Though the absolute temperature coefficient of the silicon-chromium resistors used in the AD7570 is about $-150\text{ppm}/^\circ\text{C}$, they track to within $\pm 2\text{ppm}/^\circ\text{C}$; the result is an overall gain tempco better than $10\text{ppm}/^\circ\text{C}$.

HOW THE AD7570 WORKS

Figure 28 is a functional diagram of an AD7570, connected for 10-bit unipolar A/D conversion; Figure 29 is a typical timing diagram showing what happens at the various terminals, and the sequence. (If you are perplexed about the designation or function of any of the terminals, Figure 3 and the table on the next page may be helpful.)

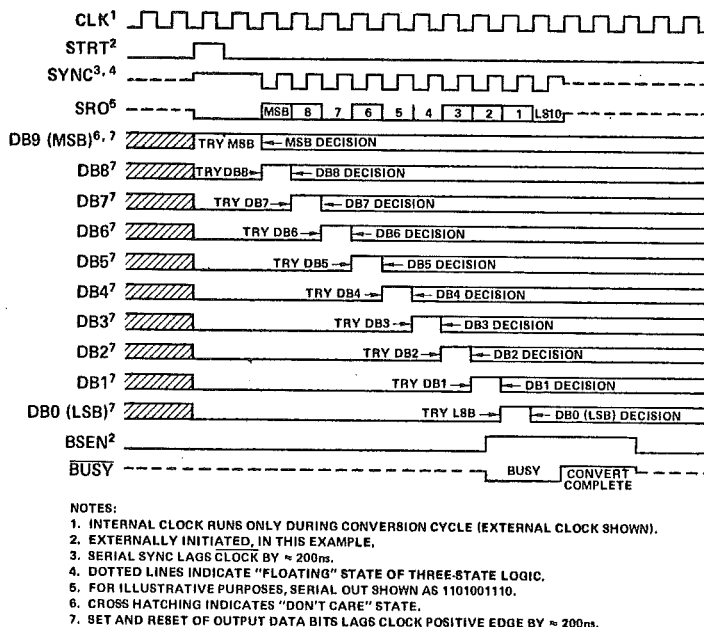


Figure 29. AD7570 timing sequence with externally-initiated start, clock, and $\overline{\text{BUSY}}$ -ENABLE, and parallel outputs continuously enabled.

In the successive-approximations technique (Chapter II-1) the output of a D/A converter is compared against the analog input for a succession of combinations of digits. When the *start* signal is given, the MSB latch output (appearing at DB9, if enabled) goes high and causes the DAC to apply a current equal to one-half of full-scale to the input network, where it is compared with the current developed by the input voltage. If the input is less, the comparator output causes the MSB latch to go low at the 2nd clock pulse plus 200ns; if the input is greater, the MSB stays high, retaining the DAC output at one-half full scale. In either case, the decision initiates the trial of the second bit ($1/4$ full scale); it is compared and accepted (input $> 1/4$ or $> 3/4$) or rejected (input $< 1/4$ or $< 3/4$). The comparison proceeds until the LSB has been tried and accepted or rejected. The outputs DB9 through DB0, if all bits are enabled, will indicate a valid binary representation of the magnitude of the analog input, relative to the reference. This result will remain latched until another conversion is initiated.

From the timing diagram, it can be seen that when convert start (STRT) goes high, DB9 is set while DB0 through DB8 are reset. Two-clock-pulses-plus-200ns after the STRT pulse returns to low the MSB (DB9) decision is made. Each succeeding trial and decision is made at $T_{\text{clk}} + 200\text{ns}$ (a fixed delay time designed into the AD7570 to ensure that data from the comparator is available at the "data" input of the output latch before clocking the latch). The output data lines (DB0 through DB9) are buffered from the output data latches by three-state drivers (similar to transmission gates in series with the outputs). The transmis-

sion gates are controlled by HBEN (High Byte ENable), which controls DB9 and DB8, the two most-significant bits, and LBEN (Low Byte ENable), which controls DB7 through DB0, the 8 least-significant bits.

The time relationship of the other signals is shown in Figure 29; their meaning and functions are explained in the table.

NOTES ON LOGIC FUNCTIONS

Inputs

- Convert Start (STRT -pin 25): When STRT goes *high*, the MSB data latch goes *high*, all other bits go *low*. Conversion begins when STRT goes *low* (at least 500ns later). If STRT is re-initiated *during* conversion, the conversion sequence starts over.
- High Byte Enable (HBEN-20): When HBEN is *low*, output lines for data bits 9 and 8 (MSB and 2nd bit) float. When HBEN is *high*, digital data from the latches appears on the data lines.
- Low Byte Enable (LBEN-21): Same function as HBEN, bits 0 (LSB) -7.
- Busy Enable (BSEN-27): When *high*, requests status of conversion (see "Busy" under Output functions).
- Short Cycle, 8 Bits ($\overline{SC8}$ -26): When *low*, conversion stops after 8 bits (essential for J); when *high*, conversion runs for 10 bits.
- Clock (CLK-24): External clock (TTL/DTL or CMOS) may be applied here. For internal clock, connect RC as shown in Figure 28 ($f \cong 2.5/RC$); clock begins with STRT, ceases at end of conversion.
- V_{DD} (VDD-1): Principal supply voltage, nominally +15V
- V_{CC} (VCC-22): Compatible logic supply; +15V: CMOS, +5V: DTL/TTL

Outputs

- Busy (\overline{BUSY} -pin 28): Indicates conversion status. Floats when BSEN-27 is *low*. When interrogated (BSEN *high*): goes high when conversion complete, stays low while conversion in process.
- Serial Output (SRO-8): Indicates state of each decision (non-return-to-zero) as conversion proceeds. Must be used with SYNC-9 for correct interpretation of data. Floats when no conversion.
- Serial Synchronization (SYNC-pin 9): Provides 10 positive edges when SRO data valid. Floats when no conversion.

APPLICATIONS

The AD7570 has many uses in standard 10-bit conversion applications. Of especial interest for microprocessor applications are the tri-state output logic and "byte-size" enabling logic. Typical applications with microprocessors are similar to those suggested for the AD7550 in Chapter I-4.

However, the AD7570's analog flexibility, achieved through a design that permits the use of external reference and comparator function, makes possible an interesting variety of applications; as examples, we will consider some resistance-measurement functions.¹⁰

Resistance Deviation

Figure 30 shows a basic configuration in which the AD7570 is used to measure the deviation of an unknown resistance from a standard and convert it to offset binary. The measurement accuracy is independent of the reference-voltage accuracy, since the measurement is performed ratiometrically.

A standard resistance, which is twice the nominal value of the unknown, is the input resistor of an inverter, and the unknown is connected as the feedback resistor. The resistance of the unknown can be expressed as $R_S (1 + \alpha)$, where α is the fractional (\pm) deviation from

¹⁰ Whitmore, J. "Resistance-Ratio-to-Digital Conversion," *Analog Dialogue* 9-3, 1975.

the nominal resistance, R_S . The output of the inverter is

$$E_1 = -\frac{R_X}{2R_S} V_{REF} = -\frac{V_{REF}}{2} (1 + \alpha) \quad (2)$$

The digital output of the A/D converter will be a fractional binary number between 0 and $(1 - 2^{-10})$ of full-scale, representing the ratio,

$$D = \frac{1}{2}(1 + \alpha) = \frac{1}{2} + \frac{1}{2}\alpha \quad (3)$$

If $\alpha = 0$, the digital output number will be 10000 00000 = $\frac{1}{2}$; if $\alpha = +\frac{1}{2}$, the digital output number will be 11000 00000 = $\frac{3}{4}$; and if $\alpha = -\frac{1}{2}$, the digital output number will be 01000 00000. It is readily seen that these values correspond to an offset-binary code that reads α directly as a bipolar number. If the MSB is complemented, the output reading will be in 2's complement coding – for $\alpha = 0, \frac{1}{2}, -\frac{1}{2}$, the codes are 00000 00000, 01000 00000, and 11000 00000, irrespective of the value of V_{REF} .

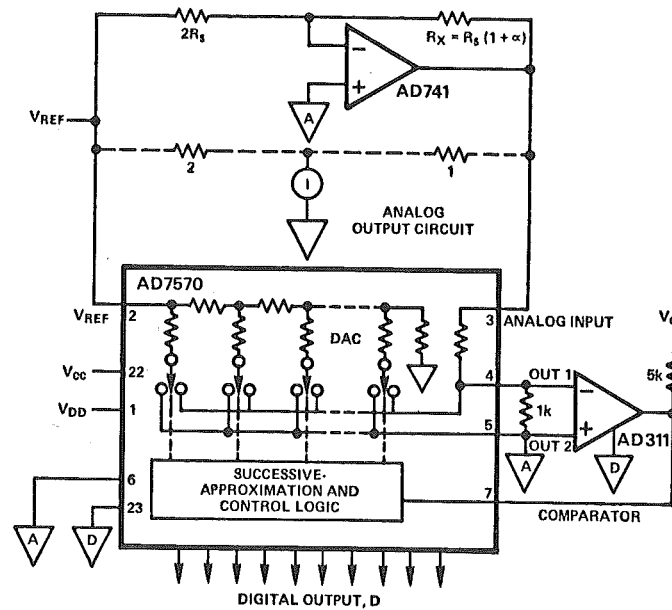


Figure 30. Resistance deviation measurement with binary output, using AD7570 A/D converter. Digital and "housekeeping" circuitry omitted for clarity.

Analog readout may also be provided in the conventional way, by the use of a precision resistance half-bridge, shown in dashed lines. The "null-meter" may be replaced by an op amp for amplification of the null signal. For digital readout with greatly-increased sensitivity, a converter may be connected in the standard bipolar-conversion configuration, to read this amplified error directly with high sensitivity.

Direct Resistance Measurement¹¹

Figure 31 shows a basic configuration in which the analog output of the D/A converter (in the successive-approximations AD7570) is converted to voltage proportional to the digital number, $-DV_{REF}$. This voltage is applied as the A/D converter input. It and the reference voltage are applied to R_X and R_S in series. The comparator acts like an op amp; that is, through the successive-approximation process, it forces the digital number, D , to be whatever value will bring the summing-point voltage, V_S , to within 1 least-significant bit of ground. Thus, at balance, with $V_S \cong 0$,

$$\frac{DV_{REF}}{R_X} = \frac{V_{REF}}{R_S} \quad (4)$$

¹¹ See Also, "Simple A/D Converter Circuit Measures Resistance Digitally," by J. Whitmore, *Electronics*, Oct. 2, 1975.

and

$$D = \frac{R_X}{R_S} \quad (5)$$

irrespective of V_{REF} . This scheme can be used to measure any value of R_X less than R_S to within 1LSB of 10 bits, or 1 part in 1024 of R_S , i.e., if $R_S = 10k\Omega$, R_X may be any value from 10Ω to $9,990\Omega$, measured with a resolution of 10Ω . The voltage, $-DV_{REF}$, may be used as an analog output.

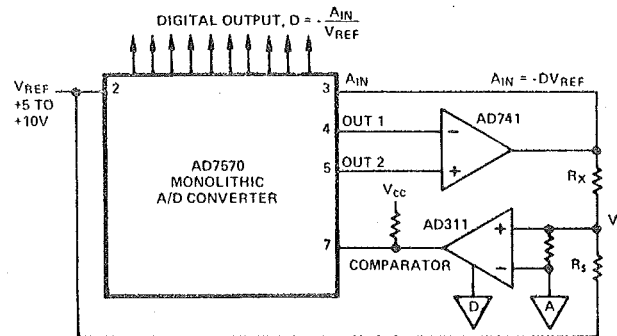


Figure 31. Direct resistance measurement. Digital output is equal to the ratio of R_X to R_S , independently of V_{REF} .

AD7550 – 13-BIT CMOS μ P-COMPATIBLE A/D CONVERTER^{1 2}

The AD7550 is a 13-Bit A/D Converter on a single 3 x 3.2mm (118 x 125 mil) chip, enclosed in a 40-pin dual in-line package (Figure 32). It utilizes a "Quad-Slope" integration technique†, which provides both autozeroing and low sensitivity to component error, supply variations, and temperature changes. It accepts analog inputs of either polarity; the output is available as either a train of pulses for external counting, or as a parallel 2's-complement word, divided into 5- and 8-bit bytes, and buffered by 3-state logic especially suited for microprocessor-controlled bus-oriented systems. The AD7550 interfaces directly with either TTL or CMOS logic.

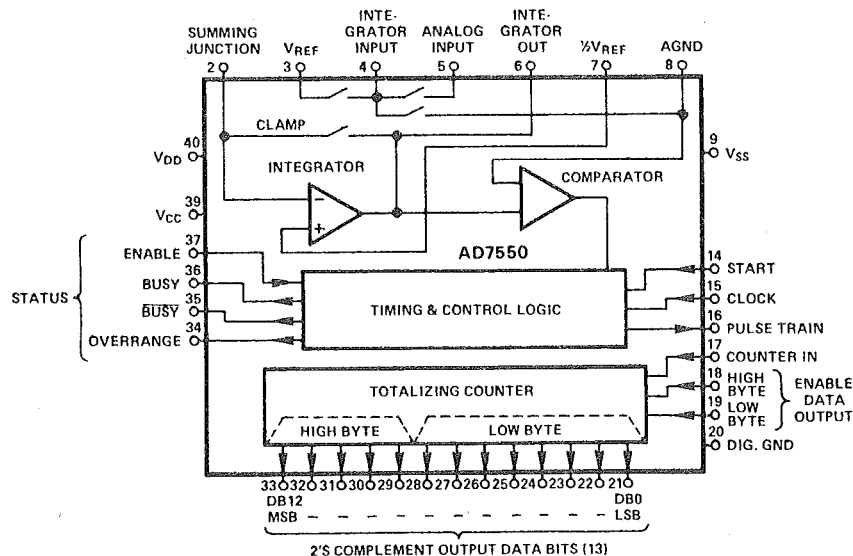


Figure 32. Block diagram of the AD7550 A/D converter.

Requiring typically only 8mW total power ($V_{DD} = 12V$, $V_{SS} = -5V$ to $-12V$, and $V_{CC} = 5V$ up to V_{DD}), and a single external positive reference, the AD7550 contains its own comparator, integrating amplifier, clock, control-, counting-, and buffer logic, and analog switches. Since

^{1 2} Ritmanich, W., Langley, D., and Wold, I., "13-Bit Monolithic CMOS A/D Converter," *Analog Dialogue* 10-1, 1976.

†U.S. Patent 3,872,466.

the reference is applied externally, the AD7550 may be used for ratiometric conversion. The internal clock may be overridden by an external clock for applications in which an external clock is desirable. The only passive external components normally required are a resistive divider-pair for the reference and a resistor-capacitor pair for the integrator (Figure 4).

Because of the integrating technique used, the digital output is monotonic, with no missing codes. The AD7550 will accurately digitize signals from up to slightly less than one-half the maximum reference down to levels limited only by the internal FET-input amplifier's ability to accurately integrate small microvolt-level signals without errors due to noise. Because the Quad-Slope integration technique accurately adjusts for offsets over the temperature range, the zero-drift and gain-temperature coefficients are less than 1ppm/°C maximum, at typical conversion speeds of 40Hz, with $\pm\frac{1}{2}$ LSB differential nonlinearity.

MICROPROCESSOR COMPATIBILITY

The AD7550 was specifically designed to be easy to use in data-bus systems, where its 3-state outputs are under external control. In this respect, the timing-sequencing and data-bus connections are compatible with those of the AD7570 and the AD7522.

- The positive-true parallel data outputs (bits 0–12), the overrange indication, and the conversion status lines (BUSY, $\overline{\text{BUSY}}$) are 3-state and are isolated from the common data bus until appropriate interrogation signals are received (Data ready? High byte? Low byte?)
- The five most-significant bits (including the sign bit), the 8 least-significant bits, and the three status bits can be interrogated in separate bytes; all 13 bits can be furnished on an 8-bit common data-bus in 2 bytes.
- The serial-output pulse stream is brought out on a separate pin with regular (TTL or CMOS) logic levels; this permits the data to be manipulated before being clocked into the output buffers. The pulse train, C_{OUT} , is activated after the completion of the measurement cycle and has a number of counts:

$$\text{C}_{\text{OUT}} = 4096 + 8704 \frac{A_{\text{IN}}}{V_{\text{REF1}}} \quad (6)$$

- If the control inputs are connected to the appropriate logic levels, the AD7550 will work as a conventional 13-bit parallel-binary A/D converter.

APPLICATIONS

The AD7550's *forte* lies in applications for which accuracy and lack of discontinuities (such as missed codes), especially over wide temperature ranges, are vastly more important than speed of conversion. The self-contained nature of the AD7550, its low power consumption, and its insensitivity to temperature and supply voltage make it ideal for use in compact, battery-powered precision instrumentation, for example, in seismic or geological exploration. On the other hand, its special control features allow it to be readily employed in microprocessor-controlled data-acquisition systems where 13-bit accuracy, flexible polarity, and a noise-averaging capability are necessary and high speed isn't.

Panel-meter and digital-voltmeter applications, especially in conjunction with a requirement for binary data for system use, and where high accuracy at elevated temperatures is necessary, are also pregnant possibilities. The count-out/count-in feature permits the pulse count to be manipulated separately (for auxiliary BCD displays), or prior to being counted in the tri-state-buffered counter (for example, by the use of binary rate-multipliers).

Figure 4 shows the basic circuit connection for binary operation. With all the data-output command inputs held high, as shown, parallel data will be present at the outputs. By selectively exercising the various command inputs — as discussed in Chapter I-4, Figs. 12 and 13 — HBEN (High Byte ENable: 5 most-significant bits), LBEN (low Byte ENable: 8 least-significant bits), and STEN (STatus ENable: OVER RanGe, BUSY, $\overline{\text{BUSY}}$), the desired data can be made available on an 8-bit data bus. The internal clock can be employed simply by replacing the 1MHz clock-input lead by a capacitor from the CLoCK terminal to ground.

Similarly, repetitive auto-start can be gained by connecting a capacitor from the STaRT terminal to ground.

3½-DIGIT DPM (0 TO +2V FULL SCALE)

Figure 33 shows a simple circuit to provide 3½-digit readout for positive input voltages. The number of output pulses is divided by 2, and the reference is scaled so that 1999 of the 2047 output pulses clock a National MM74C928 counterlatch-display through a 0 to +1.999V range.

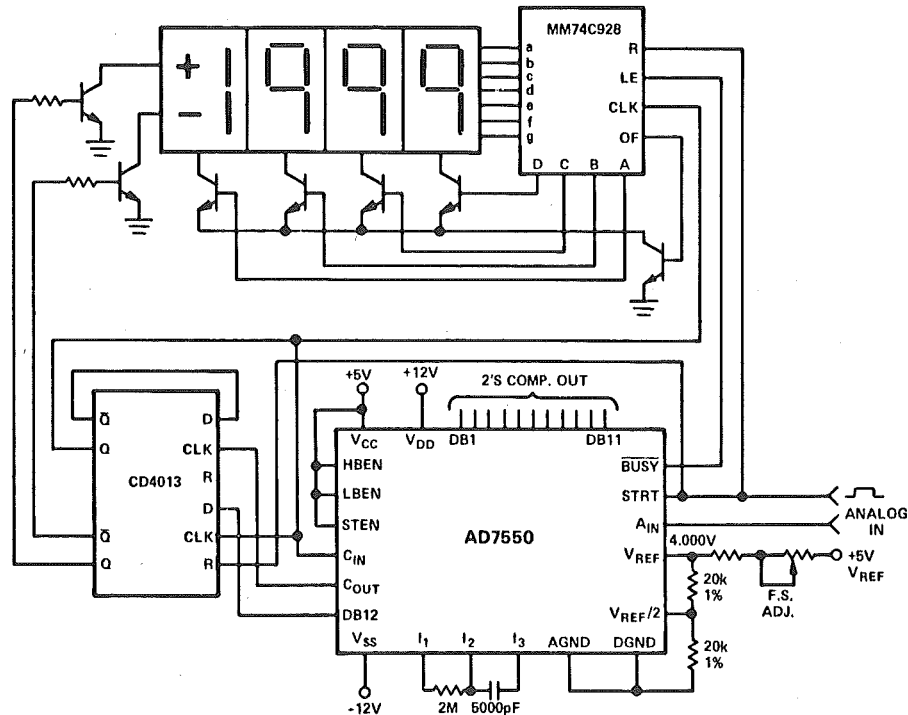


Figure 33. 3½-digit display application.

Conversion begins when the STaRT command is initiated. When DB12 goes low, indicating a positive input, the MM74C928 starts its count, corresponding to the analog input voltage. After the last COut pulse, BUSY goes high and latches the display. The Carry output of the MM74C928 indicates overrange by toggling the CD4013 to blank the display for inputs $\geq 2.000V$.

HOW THE QUAD-SLOPE CONVERTER WORKS

The quad-slope converter is an integrator-counter converter, related to the conventional dual-slope converter. However, it includes two additional integration phases for virtual cancellation of offset- and scale-factor errors by digital subtraction. Its operation can be seen in Figure 34.

The integrator has four modes of connection, determined by internally-controlled CMOS switch settings: Clamped (when no conversion is in process), Grounded input, Reference input, and Analog (signal) input. The positive input of the integrating amplifier is continuously connected to $V_{REF}/2$. When a conversion is initiated (phase "0"), V_{REF} is applied to the integrator input, providing a net positive voltage, $V_{REF} - V_{REF}/2$, across the integrator's input resistor, resulting in a negative-going ramp at the output. When the output is equal to the comparator trip-voltage, Phase 1 is initiated.

Phase 1. The integrator input is connected to Analog Ground. Since the integrating resistor has a net negative voltage across it, equal to $-V_{REF}/2$, plus any error, the output increases positively at a proportional rate. At the beginning of Phase 1, a counter starts counting clock pulses. When it has counted a number of pulses representing an interval, $T/2$, Phase 2 is initiated; the counter continues to count.

Phase 2. The integrator input is connected to the Reference. Since the voltage across the integrating resistor is $+V_{REF}/2$, plus any error, the output ramps down at a proportional

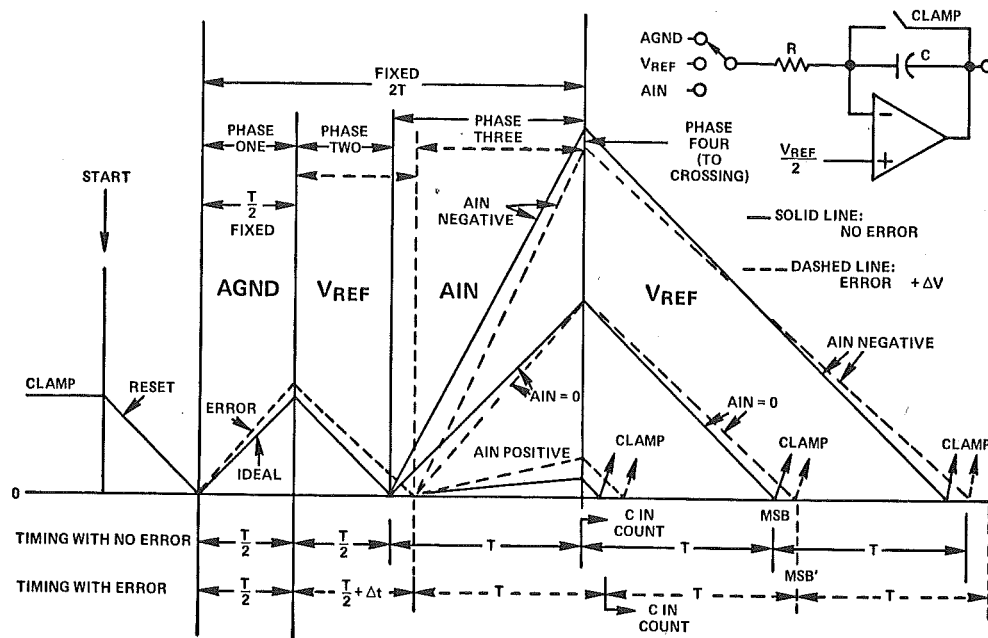


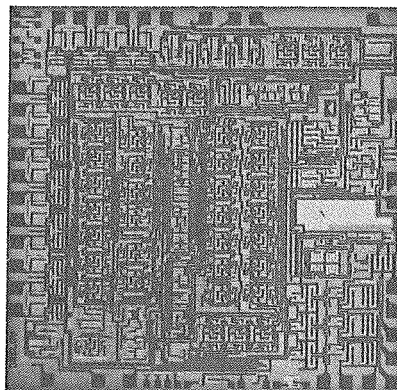
Figure 34. Illustration of quad-slope principle: integrator output waveforms for positive, negative, and zero input – with and without error.

rate. When the output reaches the comparator trip voltage, Phase 3 is initiated. If there were no error, the time for Phase 2 would be equal to $T/2$, the same as for Phase 1. Any error will increase or decrease the time to the trip point by an amount Δt . Note that the trip point is approached with the same slope and from the same direction as at the end of Phase 0 (and also the end of Phase 4), hence any comparator hysteresis errors and differential propagation delays are avoided.

Phase 3. The integrator input is connected to the Analog signal, which is positive or negative, and less than $V_{REF}/2$ in magnitude. The net input to the integrator will always be negative and equal to $A_{IN} - V_{REF}/2$, plus any error. The output of the integrator will ramp upwards with a proportional slope. For large positive inputs, the output slope will be small; for large negative inputs, the output slope will be steep; and for zero input, the slope will be the same as in Phase 1. Phase 3 is terminated when the counter that started at the beginning of Phase 1 reaches a count corresponding to $2T$.

Because Phases 1, 2, and 3 occupy a total period $2T$, Phase 3 is lengthened or shortened by Δt , the same amount by which Phase 2 was shortened or lengthened. At the *beginning* of Phase 3, a second counter is starting, counting *down* from zero*; note that, with zero error, it starts at T exactly; but with an error, it starts at $T \pm \Delta t$.

Phase 4. The integrator input is again connected to the Reference, and it ramps down at the rate $V_{REF}/2$, plus any error. Phase 4 ends when the integrator output reaches the trip point,



*The implementation discussed here is simplified for clarity.

after which the integrator is clamped and the second counter is stopped. Conversion is now complete, and the counter output is a 2's complement representation of the analog input.

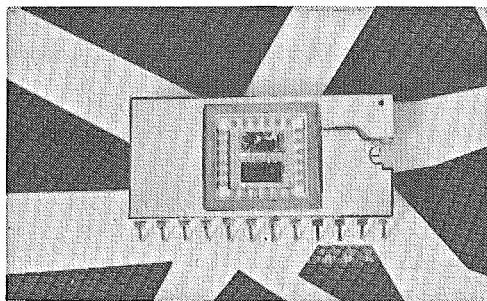
Discussion. The data sheet describes the actual workings of the circuit in some detail and includes a derivation of the error equation, which indicates square-law weighting, making small errors much smaller. Here we will rely somewhat more on graphics and intuition to show that it actually works. In Figure 34, it can be seen that the time from the MSB crossing, corresponding to zero input, to the time of occurrence of the crossing corresponding to a positive or a negative input, is proportional to that input. The effect of an error is simply to shift *all* crossings by an equal amount of time, Δt .

If the counter's capacity is $2T$, and if it counts down from all zero's at the beginning of Phase 3, then at the largest positive number, it will read 0 1111 1111 1111 (and will stop there if a crossing occurs), at zero it will read 0 0000 0000 0000, and at the largest negative number, it will read 1 0000 0000 0000, a range which will be recognized as belonging to a 2's-complement code.

In actual practice, in order to avoid negative integration and allow sufficient time after Phase 4 begins for offset correction and overrange indication, a somewhat different counting scheme is used, in association with an input full-scale range of $V_{REF}/2.125$, instead of $V_{REF}/2$.

THE AD562—12-BIT DIGITAL-TO-ANALOG CONVERTER¹³

The AD562 is a 12-bit integrated-circuit digital-to-analog converter in a hermetically-sealed 24-lead ceramic dual in-line package; it is available in both binary and BCD versions. Monotonic 12-bit resolution is guaranteed over the operating temperature range, with less than $\frac{1}{2}$ LSB ($\frac{1}{4}$ LSB for AD562S) *max* total error at $+25^{\circ}\text{C}$, and $3\text{ppm}/^{\circ}\text{C}$ *max* gain-temperature coefficient. The circuit assembly consists of two interconnected chips: (1) a monolithic bipolar transistor chip, which contains the 12 precision current switches, and (2) a compatible Si-Cr thin-film resistor chip, with the bit-weighting and range-setting resistors. All scale factors are accurately calibrated by computer-controlled automatic laser-trimming of the resistors while the device is operating — the key to its outstanding resolution and calibration accuracy, as well as its low price.



The AD562 (Figure 5) accepts an external analog reference voltage (0 to $+10\text{V}$) and supplies a binary-weighted output current proportional to the product of the 12-bit digital input-code and the value of the reference voltage, which can be either fixed or variable. When the reference is fixed, the AD562 functions as a normal DAC. When V_R is a variable unipolar (0 to $+10\text{V}$) voltage, the device is a 2-quadrant multiplying DAC; the digital input code can be either unipolar (binary or BCD) or bipolar (offset binary). The AD563 D/A converter, which contains an AD562 (scaled for 2.5V reference) and a 2.5V reference, was designed for applications calling for a 12-bit fixed-reference DAC in a single IC Package.

Nominal full-scale output current (unipolar mode) is -2mA . Internally-trimmed gain-, voltage-range-, and bipolar-offset-resistors are incorporated, to provide precise voltage outputs via an external op amp. Since all voltage scale-factors rely on resistance

¹³ Craven, R. and Harris, S., "12-Bit Integrated-Circuit D/A Converter," *Analog Dialogue* 8-2, 1974.

ratios, their temperature coefficients are determined by tracking TCR's (about 1ppm/°C) rather than absolute TCR's (about -30ppm/°C). With $V_R = +10V$, the following voltage ranges can be pin-programmed (see Figure 36): 0V to +5V, -2.5V to +2.5V, 0V to +10V, -5V to +5V, -10V to +10V. The AD562's current output, when used with the internal ranging resistors, allows the device to be used as the D/A weighting element in both voltage-output DAC's and voltage-input ADC's, with very low voltage-gain T.C., because these resistors track the other thin-film network resistors to better than $\pm 2\text{ppm}/^\circ\text{C}$.

Logic Inputs. The logic relationship is "positive-true": voltage above threshold ("1") turns a bit *on*; voltage below threshold ("0") turns it *off*. Logic drive currents are only $-100\mu\text{A max}$ at "0" and $+100\text{nA max}$ at "1", values compatible with both CMOS and TTL logic. Pin 2 sets the internal logic threshold for the digital inputs, bits 1–12. When it is open-circuited, with $V_{CC} = +5V$, the threshold is approximately +1.4V, and the device is TTL-compatible. For CMOS, pin 2 is externally connected to pin 1; the internal logic threshold is thereby set at $\sim V_{CC}/2$, and the device is then fully compatible with both low- and high-voltage CMOS, over the range $+4.75V \leq V_{CC} \leq +15.8V$.

Coding. The various voltage ranges that can be pin-programmed are shown in Figure 35. For bipolar ranges, a fixed current is subtracted from the output current to

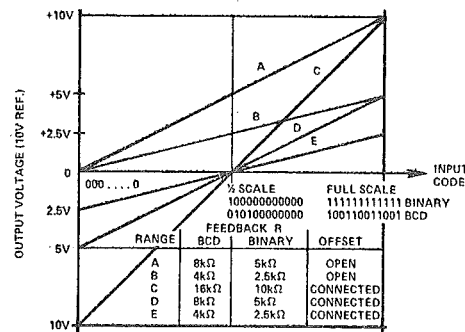


Figure 35. Voltage vs. digital input code for various connections of span and bipolar-offset resistors (10V reference).

offset it by half-scale, by the connection of the other end of the bipolar offset resistor (through an external trim pot) to V_R (Figure 36). Analog voltage zero occurs at digital code 1000 0000 0000 (2048/4096 of F.S. span) for binary models, and at 0101 0000 0000 (500/1000 F.S.) for BCD (binary-coded decimal) models.

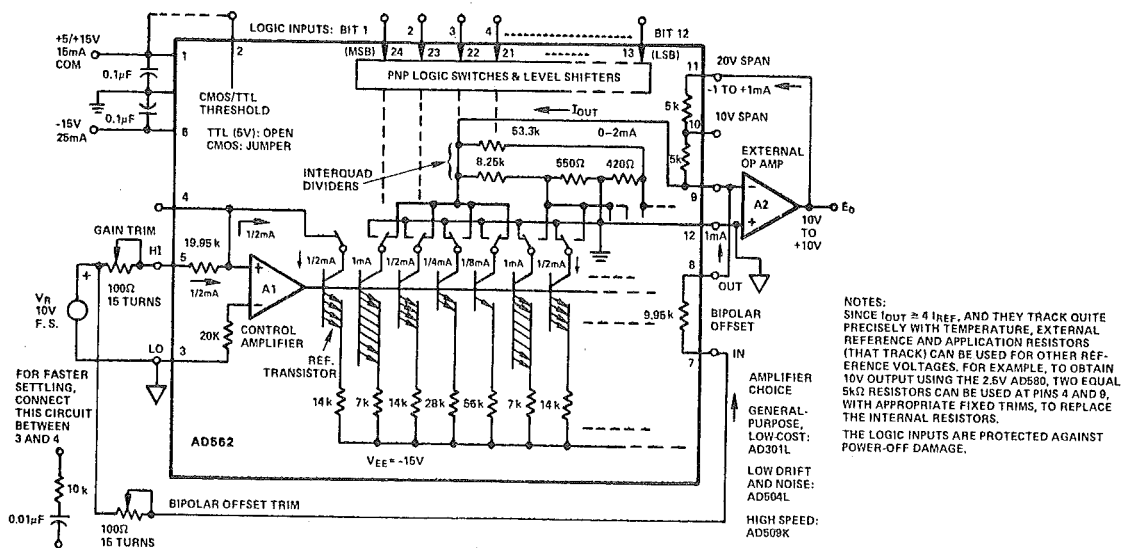


Figure 36. Functional schematic of the AD562.

CIRCUIT DESIGN

The AD562 current output is the weighted sum of the outputs of three similar groups of binary-scaled quad current-generators, controlled by V_R . The logic inputs steer these currents through non-saturating bipolar-transistor current switches to either ground or the respective quad output bus. Output currents from the 2nd and 3rd quads are attenuated (in effect) by 16:1 and 256:1 (binary; 10:1 and 100:1 for BCD), and summed with the unattenuated output of the first quad. The output current is thus the sum of 12 individually-switched currents having a binary relationship. Figure 36 shows the overall scheme. Figure 37 shows the simplified details of the control amplifier, constant-current transistors, and switching-cell interconnections.

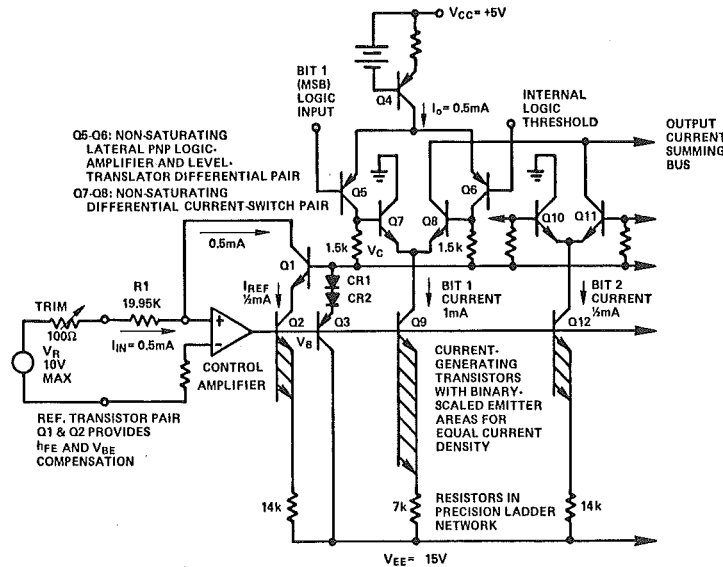


Figure 37. Control amplifier, current generators, and bit-switching cell structure.

The current-generating transistors (Q9, Q12, etc.) of each quad group have emitter areas in the ratio 8:4:2:1. The ladder-network resistances between the emitters of Q9, Q12, etc. and the -15V supply are in the ratio 1:2:4:8 (bits 1, 2, 3, 4 in the first quad). With equal voltages applied to the resistors, the emitter currents of Q9, Q12, etc., are therefore in a binary ratio. Because of their weighted emitter area, these transistors operate at equal emitter-current densities and therefore have nearly-equal V_{BE} 's and h_{FE} 's. The control amplifier (A1) drives the bases of the constant-current transistors and also a reference-transistor pair (Q2—Q1), which has h_{FE} and V_{BE} matched to those of the constant-current (Q9, Q12, etc.) and bit-switching (Q8, Q11, etc.) transistors.

V_R is applied to the externally-trimmed gain resistor R1 to set a reference current, $I_R = 10V/20k\Omega = 0.5mA$ F.S.). Amplifier A1 establishes the appropriate base voltage to force Q1 collector current equal to I_R . Variations in h_{FE} , V_{BE} , or supply voltage with time and/or temperature are sensed in the reference-transistor pair. The control amplifier then adjusts V_{BE} to hold Q1 collector current (and therefore the bit currents) constant in the presence of these variations. The use of Q1, Q2, and A1 reduces the net gain T.C. to a function of the differential h_{FE} and V_{BE} between the monolithically matched reference- and bit-switching-pairs. This close match results in an overall transistor-contribution of $<1ppm/^{\circ}C$ to the gain T.C.

Output current (for example, Bit 1) is switched by steering Q9's collector current either to ground through Q7, or to the output through Q8. With Bit 1 *high*, Q5 is turned off, and I_O is steered through Q6; Q8 is turned on, Q7 is turned off, and Q9 collector current flows through the output. With Bit 1 *low*, Q6 is turned off, and I_O is steered through Q5; Q7 is on, Q8 is off, and the Q9 collector current flows to ground. This fully-differential switching takes place rapidly, since there is no change in steady-state voltage at the emitters of Q7—Q8, with a speed that is *nearly independent of the current level being switched*. (Switching

speeds for most commercially-available DAC's vary significantly as a function of current level.) This feature is particularly useful in multiplier applications, which require fast switching at reduced (as well as full-scale) current levels, as a function of V_R .

The excellent V_{BE} match (to about 1mV) of Q2, Q9, Q12, etc., permits accurate multiplication (fast or slow) at reduced current levels (V_{BE} mismatch among the output-current switch transistors, Q8, Q11, etc., which are cascode-connected, does not affect bit-weighting accuracy).

Since the collector voltage of Q2, Q9, Q12, etc., does not change during bit switching, there is no differential power change as various bit combinations are switched. Moreover, the four most-significant current-setting transistors (Q9, Q12, Q15, Q18) are located on the axis of symmetry between Q7–Q8, Q10–Q11, etc., virtually freeing the device from nonlinearity and thermal-transient errors attributable to differential heating. Typical AD562 nonlinearity is, in fact, less than 30ppm F.S.

Q3 and diodes CR1 and CR2 form a bootstrapped bias source which causes the voltage V_C (very nearly equal to the collector voltages of Q9, Q12, etc.) to track the base voltage V_B . The collector-base voltage of Q9, Q12, etc., is thus maintained at approximately $3V_{BE}$, irrespective of supply- or reference-voltage variations (which are impressed across the switch transistors instead). Bootstrapping prevents h_{RE} effects from introducing errors into the bit currents and contributes to the AD562's excellent supply-voltage rejection and multiplier performance.

APPLICATIONS

Multiplication. As noted above, the AD562 can be used as a multiplying DAC. The analog input (V_R) must be unipolar (0 to +10V); the digital coding may be either unipolar (single quadrant) or bipolar (2 quadrants). When V_R is +1V (10%F.S.), worst-case error is only about 0.05% of the (reduced) full-scale output. Settling time for a 10V-full-scale V_R step is $5\mu s$ to 0.01%, while the slewing rate is $1mA/\mu s$ (or $5V/\mu s$ with a suitable output amplifier providing a 0–10V range), with all bits *on*. Feedthrough of a full-scale (10Vp-p) sinewave, with all bits *off*, is 0.0125%F.S. at 2kHz, increasing at 20dB/decade at higher frequency.

12-Bit Successive-Approximations A/D Converter (Figure 38). The AD562 is shown here as the D/A weighing element in a 12-bit ADC, for conversion rates up to 40kHz. The digital output-equivalent of the analog input is formed by weighing the programmed DAC-output, one bit at a time (MSB first, LSB last), and accepting or rejecting each bit, depending upon

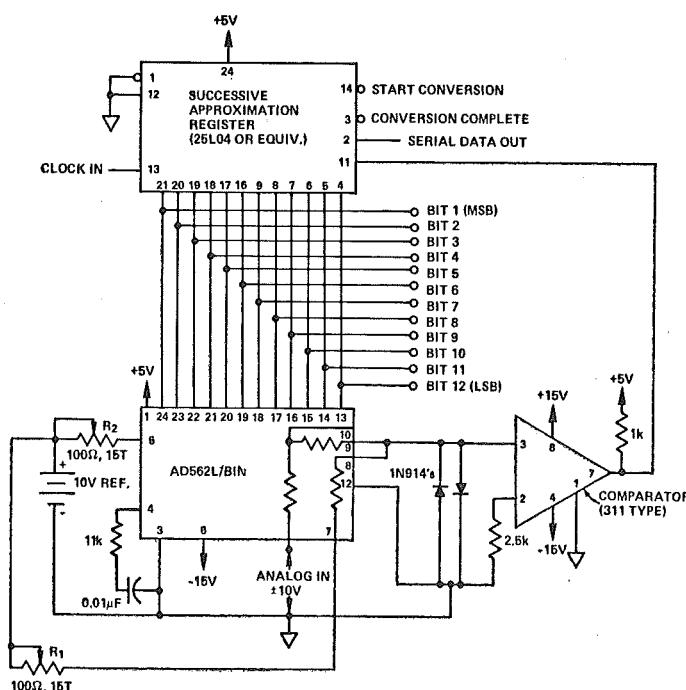


Figure 38. 12-bit successive approximation A/D converter.

the comparator state following each bit-trial. The analog input voltage is applied to the appropriate AD562 span resistor, and the current-output terminal (summing-point) voltage is compared against "ground." The AD562's output voltage is diode-clamped to keep the out-of-balance error voltage within the device's compliance-voltage limits. The AD562's multiplying capability permits the reference voltage to be varied for ratiometric conversion. It should be noted that the AD562 is at the heart of the AD572 A/D converter.

AD561 HIGH-ACCURACY 10-BIT DAC WITH BUILT-IN REFERENCE¹⁴

The AD561 is a 10-bit single-chip digital-to-analog converter in a 16-pin ceramic DIP; it contains its own high-stability voltage reference. In response to a positive-true TTL or CMOS parallel digital input, it produces a high-compliance (-2V to +10V) 0 to 2mA current output. Completely self-contained are the reference, R-2R thin-film-on-silicon ladder network, current-steering switches, and the application resistors needed for generating high-precision $\pm 5V$ and 0 to +10V outputs, when used with an output buffer amplifier. The AD561 has the best guaranteed accuracy at 25°C ($\frac{1}{4}LSB_{max}-K,T$) and the tightest tempco (30ppm/°C *max*) among known 10-bit IC D/A converters, and it is the *only* such IC to be guaranteed monotonic over the operating temperature range (0°C to 70°C-J,K; -55°C to +125°C-S,T). As a further bonus, full-scale settling time to within $\frac{1}{2}LSB$ is 250ns.

As of this writing, not only is the AD561 the most-accurate and stable in its class — it is also one of the *least-expensive* 10-bit D/A converters available!

PROCESS LIMITATIONS

Until the AD561 became available, an appropriate IC with the right combination of accuracy and cost had not been available to system designers who needed true 10-bit (0.1%) device accuracy.* The various options theretofore available — none of them attractive — ran the gamut from the compromises inherent in untrimmed, low-priced 10-bit converters to adequate (but expensive) 10-bit hybrids to overdesign by the use of 12-bit converters (to be sure of adequate 10-bit performance at the extremes of temperature). Semiconductor manufacturers had consistently found that it was well-nigh impossible to obtain substantial yields of IC's containing a resistive ladder network, with matching and tracking properties adequate for a 0.1% device, by the use of the photolithographic process alone (and low yield = high cost).

The key to overcoming these linearity limitations, using today's technology, is to laser-trim the resistor networks *and* the reference tempco *at the wafer stage*, a process developed as a cost-effective manufacturing tool at Analog Devices Semiconductor.¹⁵ The thin-film R-2R ladder network is trimmed by a high-resolution laser-trimming system to provide conversion linearity of the order of 0.01%. These devices, which have been trimmed at the wafer stage, are then assembled, sealed, and burned-in, after which they are graded into $\frac{1}{4}LSB$ (K & T) and $\frac{1}{2}LSB$ (J & S) categories. This system adds the benefits of high yield to the already traditionally low IC-manufacturing costs.

BURIED REFERENCE DIODE

The key to the AD561's overall gain accuracy is the stable reference. "Zener" reference diodes are easy to make on an IC chip: just use the reverse-breakdown voltage of a base-emitter junction. This technique is widely used. Unfortunately, such diodes are noisy and unstable, because the breakdown occurs at the surface of the die, where shifts of the breakdown point, caused by variations of stress produced by charged oxide impurities, especially mobile ions, can significantly affect stability. Long-term shifts of up to a few percent are not uncommon, a phenomenon hardly compatible with overall 0.1% device performance.

For the AD561, a deep-diffusion technique is used to "bury" its reference diode; the break-

¹⁴Kress, D., "Highest-Performance 10-Bit IC DAC," *Analog Dialogue* 11-1, 1977.

*For example, in an industrial measurement and control system where transducer errors may be typically 0.5% to 1%, the AD561's performance combination may be needed to avoid the introduction of significant additional error and further degradation of system accuracy.

¹⁵Wagner, R., "Laser-Trimming on the Wafer," *Analog Dialogue* 9-3, 1975.

down, occurring well below the surface, is characterized by considerably less noise and by long-term instability of only a few ppm/year. For the complete D/A converter, stability is typically within 50-100ppm/year. Stability of the reference with temperature is optimized by laser-trimming of the reference-compensation circuitry for near-zero overall drift. Combined with the close tracking of the metal-film (Si-Cr) resistors, this results in low initial calibration errors, high linearity, and low drift with temperature.

DESIGN

Figure 6 shows the complete (simplified) circuit of AD561. The buried-reference-diode circuitry develops -7.5V , which is scaled by an inverting amplifier, A1, to $+2.5\text{V}$. This voltage level permits the AD561 to operate well with positive supply voltages as low as 4.5V . The reference voltage produces an input current to inverting amplifier, A2; the 1mA current (I_{REF}) is duplicated by the control transistor, Q1, which enforces the necessary voltage between the base line and one end of the R-2R ladder. Since Q2 is identical to Q1, and its base-emitter circuit operates under exactly the same conditions, its collector current (the MSB) is also equal to I_{REF} . The state of the digital input determines whether the collector current is added to the output current via Q3 or is harmlessly shunted to ground via Q4 by the Craven-cell current-steering switch,¹⁶ described earlier (Figure 37).

A set of binary-weighted currents, produced via an R-2R ladder network, are stabilized and switched by familiar techniques (Chapter II-1) (with a few new wrinkles, explained on the data sheet). $5\text{k}\Omega$ resistors provide the full-range scaling†, and a $2.5\text{k}\Omega$ resistor, connected to the 2.5V reference, provides bipolar offset current.

APPLICATION FEATURES AND CIRCUITS

In Figures 39 and 40, the AD561 is shown connected for operation in the unipolar (0 to $+10\text{V}$) and bipolar ($\pm 5\text{V}$) output modes. The internal $5\text{k}\Omega$ and $2.5\text{k}\Omega$ resistors are pretrimmed and typically provide scale-factor and bipolar-offset accuracy to within 0.1% (0.5% max), with external 25Ω and 10Ω fixed resistors added in series. For higher absolute accuracy, variable resistances of 50Ω and 20Ω full-scale are used instead to calibrate the gain and bipolar offset.

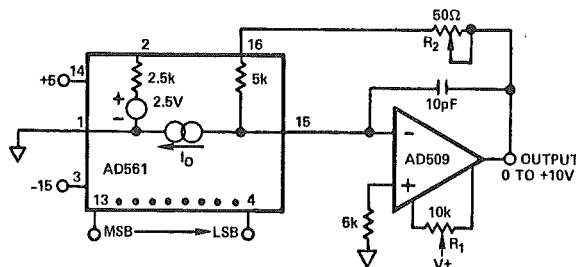


Figure 39. Connecting the AD561 for buffered 0V to $+10\text{V}$ output. The adjustment pot may be replaced by a fixed 25Ω resistor for 10mV typical output error.

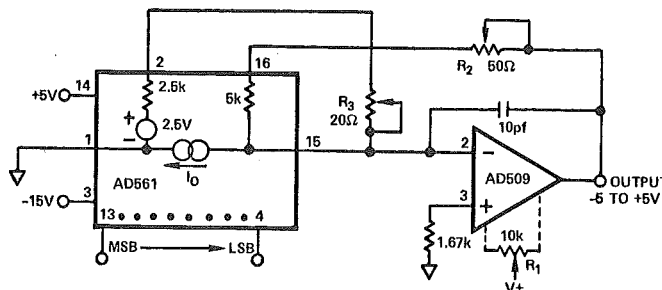


Figure 40. Connections for buffered $\pm 5\text{V}$ output. Adjustment pots may be replaced by mid-range resistances with 10mV typical error.

¹⁶U.S. Patent 3,961,326.

†Standard output range is $\pm 5\text{V}$ or 0 to $+10\text{V}$. Also available on the chip for optional bonding are: $\pm 10\text{V}$, 0 to $+20\text{V}$; $\pm 2.5\text{V}$, 0 to $+5\text{V}$.

Compliance Range. The AD561 has the widest-known compliance-voltage range available for a 10-bit IC DAC; the output is guaranteed to swing from -2V to +10V at 2mA full-scale output. The specified output impedance of (typically) $40\text{M}\Omega$ means that a 12-volt swing through the compliance range will result in an output-current change of only $0.3\mu\text{A}$ (0.15 LSB). This permits the AD561 to produce a voltage output without the use of an op amp. A resistor to ground will produce a voltage output; the parallel load resistance should be less than $1\text{k}\Omega$ in order to stay within the -2V limit. Bipolar connections are also easily accomplished, and a 0V to +10V range can be achieved by connecting the resistor to a precision 10V supply, as Figure 41 shows.

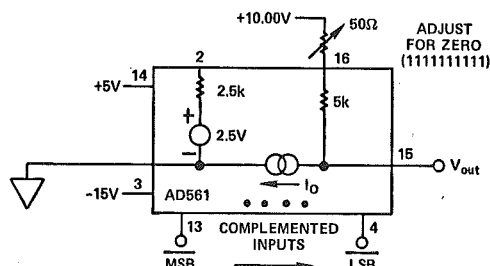


Figure 41. AD561 connected for unbuffered 0V to +10V output, with $5\text{k}\Omega$ output impedance. For this application, data inputs are negative true. Typical applications call for light load, e.g., with high-impedance devices or in null-seeking.

It should be noted that the AD561's high output impedance is what makes the wide range of compliance voltage especially useful, since the output voltage is determined entirely by the load resistance, which may be arbitrarily chosen. As an example of the problems that arise, the compliance-voltage specification of the AD561 is +10V to -1.5V, but the $8\text{k}\Omega$ typical output resistance specification means that the actual output voltage will depend, not only on the load resistance, but also on the output resistance of the device (and its 10% tolerance).

Digital Threshold. The threshold for digital input is automatically set as a function of the positive supply level. For TTL/DTL or 5V CMOS, a 5V value of V_{CC} gives a 1.4V threshold and guarantees the input limits. The thresholds for $V_{CC} = 10\text{V}$ and $V_{CC} = 15\text{V}$ are 5V and 7.5V, which provides suitable limits for the respective logic families. Since the logic inputs are high-impedance, even unbuffered CMOS can be used without difficulty.

Fast Settling. The high-speed Craven-cell output switches and critically damped control amplifier produce fast-settling performance. Worst-case settling time to within 0.05% F.S. ($\frac{1}{2}$ LSB),

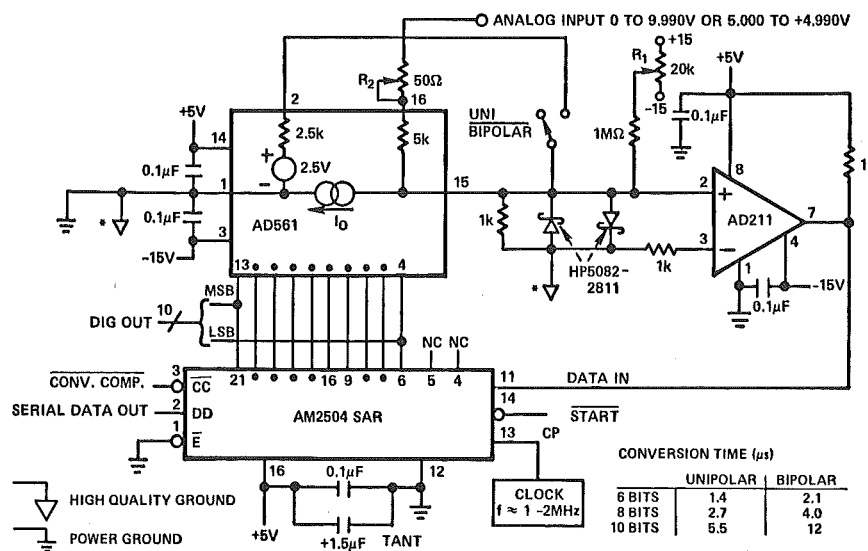


Figure 42. Fast 10-bit A/D converter. Its implementation is discussed on the AD561 data sheet.

for all-bits-off to all-bits-on is less than 250ns; the lower-order bits settle individually in less than 200ns. When the AD561 is used with the AD509 high-speed op amp, the output can be made to settle in less than 600ns. This kind of high-speed performance is useful for constructing a fast A/D converter, such as the one shown in Figure 42.

THE AD2026 PANEL METER^{1 7}

While not an IC converter, in a strict sense, the AD2026 chip design is worth discussing, for several reasons. It is the first-known use of I²L technology for a commercial conversion device (and it is still the only one that can be more-or-less freely discussed at this writing). Second, it permits the reader who is unfamiliar with I²L to gain an insight into its possibilities. Third, the underlying philosophy may be of interest.

The AD2026 is a 3-digit panel meter (DPM), powered by a single +5V supply, with 0.5" (13mm) LED display, and overall dimensions of 87 x 52 x 22mm (3.43" x 2.04" x 0.85"). Intended to supplant measurement-grade analog panel meters in new instrument designs, it provides high reliability at low cost. Achievement of these usually conflicting objectives is the culmination of a project that required innovations* in design, manufacturing, and test. Key elements include a proprietary I²L† chip that reduces total electrical parts count to 14, a single-board design that is batch-assembled and-tested, and a proprietary case that requires no tools or hardware for assembly and mounting.

Besides the design of the I²L chip (and the choice of the technology), the key factors in the cost-effective design of the AD2026 were the fundamental decisions on the features of the device — made after a thorough study of the needs of high-accuracy *analog* panel-meter users (price, display, polarity and zero, accuracy and repeatability, reliability, and size) — and the use of mass-production techniques in the fabrication of the instrument.

DESIGN

The AD2026 uses the classical dual-slope integrating A/D conversion technique. The input signal is integrated for a fixed interval of time, then a reference of opposite polarity is integrated for the time required for the integrator output to "ramp" back to its starting level. That time interval, measured by counting a train of clock pulses, is proportional to the input (and insensitive to such parameters as integrator time constant and accuracy of the clock rate).

In the AD2026, the input is offset, to permit the specified 10% negative capability (Table 1). The offset is interpreted digitally by relatively simple logic circuitry, which complements the BCD data for negative inputs and provides the minus sign in place of the "hundreds" digit. The offset input eliminates the need for two reference polarities, resulting in greatly improved linearity near zero and a saving of chip area.

INPUT	READING
>999mV	E E E
999mV	9 9 9
998mV	9 9 8
●	●
●	●
zero	0 0 0
-1mV	- 0 1
●	●
●	●
-99mV	- 9 9
<-99mV	- - -

Table 1. AD2026 output vs. input (3 decimal points selectable at connector)

^{1 7}Boole, R, and Smith, L., "Revolutionary Panel Meter Uses I²L Chip," *Analog Dialogue* 10-2, 1976.

*Patents applied for

†Integrated Injection Logic.

There are several advantages to short conversion times: No data latches are required, since the displays are blanked during conversion and unchanged at other times. In addition, LSI area is saved by using an essentially passive integrator. Also, the short conversion time reduces the size of integrating capacitor to manageable proportions. Finally, the display blanking during conversion means that interaction between the display and the converter is eliminated, which makes for outstanding differential linearity.

The block diagram illustrates the internal architecture of the LSI circuit. Key components and their interconnections include:

- Inputs:** An **INPUT** terminal and a **HOLD** terminal are shown. The **LSI CIRCUIT** is powered by a **+5** V supply and connected to **GND**.
- Reference Section:** A **BAND GAP REFERENCE** feeds into a **REFERENCE CURRENT SOURCE**, which provides a reference current to the **COMPARATOR**.
- Input Section:** The **INPUT** signal passes through a **VOLTAGE TO CURRENT CONVERTER**, which is also influenced by a **ZERO ADJUST** potentiometer. Its output is connected to the **COMPARATOR**.
- Control and Timing:** The **COMPARATOR** output goes to **CONTROL LOGIC**, which is also triggered by the **HOLD** signal. The **CONTROL LOGIC** generates a **CLOCK** signal for the **COUNTER** and a **DIVIDER CHAIN**.
- Counting and Multiplexing:** The **COUNTER** sends data to a **MULTIPLEXER**, which also receives feedback from the **COMPLEMENT CIRCUIT**.
- Output Section:** The **MULTIPLEXER** output is sent to a **TTL DECODER**, which then drives three **LED DISPLAY** units. A **COMPLEMENT CIRCUIT** also provides a direct output to one of the displays.
- Adjustments:** A **GAIN ADJUST** potentiometer is connected to the **REFERENCE CURRENT SOURCE** and the **COMPARATOR** input. An **INTEGRATION CAPACITOR** is connected to the **VOLTAGE TO CURRENT CONVERTER** output.

ISSUE	I^2L	CMOS
Yield Factors		
A) Experience	Considerable applicable analog experience.	Considerable digital experience.
B) Major cause of limited yields	Collector to emitter shorts.	Surface contamination.
C) Density	Approximately 10mils ² per gate.	Approximately 30mils ² per gate.
Analog Functions		
A) Versatility	Excellent. Possible circuits include band gap references and power.	Poor. However, good analog switches are inherent.
B) Precision	Good.	Fair.
C) Complexity	Excellent.	Fair. Present state of the art is two or three op amps.
Digital Functions		
A) Power x delay	Less than 1pJ.	Approximately 3pJ.
B) Interface	Good. Will easily sink 10 TTL loads.	Fair. TTL compatibility is possible at the expense of chip area.

Table 2. Comparison of I^2L and CMOS.

WHAT IS I^2L ?

MOS and bipolar are the two basic LSI semiconductor processes. MOS produces very dense – therefore low-cost – logic circuits but is capable only of crude analog devices. Before I^2L , bipolar could offer stable high-quality devices suitable for precision analog circuits, but logic consumed much expensive chip area.

Integrated Injection Logic (I^2L) now allows the design of single-chip devices containing both analog and digital functions, without calling for the compromises required in the past. I^2L has a logic density that equals or exceeds that of MOS, while employing a bipolar process suitable for precision analog circuitry.

I^2L eliminates the complexity of conventional bipolar logic by using inverted transistors (collectors and emitters are interchanged). Figure 44 shows a conventional transistor, with its wraparound P+ isolation region, which is needed to separate the collectors of adjacent transistors. When the transistors are inverted, the collectors are automatically isolated, and the emitters are fortuitously grounded, at the same time.

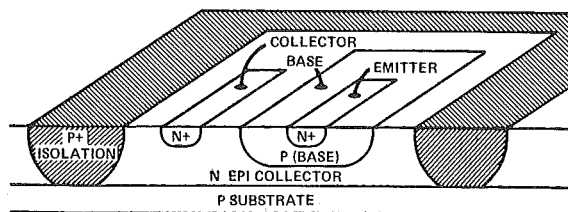


Figure 44. 3-dimensional section of conventional NPN transistor.

Since I^2L logic gates can easily have multiple outputs, it is possible to use simple “wired-or logic”, a means of implementing the logical *or* operation using only one conductor (*wire*). Figure 45a shows an example of two I^2L gates wire-or’d to implement the *nor* function.

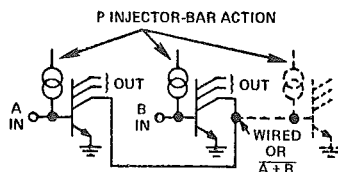


Figure 45a. I^2L gates wired to implement NOR function.

A major contributor to I^2L 's compactness is replacement of conventional “pullup” resistors or transistors by an injector bar. In Figure 45b, the P injector acts as a combined power-

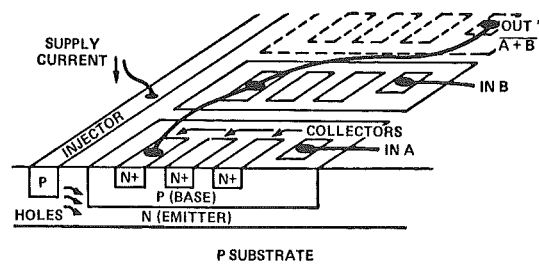


Figure 45b. Sectional view of I^2L circuit.

supply rail and current source for the I^2L gates. Holes are injected into the chip and collected by nearby base regions so as to pull-up each gate.

Analog circuitry may be placed on the same chip by using conventional transistors like that of Figure 44. Thus, I^2L can be seen to combine the possibility of high-density logic functions with precision analog circuitry.

THE AD572 – 12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide modular performance, flexibility, and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of $\pm 0.012\%$, gain T.C. below 15ppm/°C, typical power dissipation of 900mW, and conversion time of less than 25 μ s. Of considerable significance in military and aerospace applications is the guaranteed performance from -55 to +125°C of the AD572S, and the availability of units processed to MIL-STD-883B. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25 to +85°C, and -55 to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ± 2.5 , ± 5.0 , ± 10 , 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The AD572 is packaged in a hermetically-sealed, all-metal DIP. Welding-rather than solder sealing-eliminates any possibility of contamination from flux and solder particles. The metal construction provides excellent shielding from random electrostatic and/or electromagnetic radiation which could cause incorrect output codes. To insure a level of reliability consistent with its performance, each AD572 receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, acceleration testing, fine and gross leak testing, and operating burn-in.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25 to +85°C, and the "S" from -55 to +125°C.

DESIGN

The AD572 functional diagram and pin-out are shown in Figure 46. The device consists of the following monolithic bipolar transistor and thin-film-resistor circuit elements:

1. 12-bit successive-approximation register
2. 12-bit feedback DAC weighing network
3. Low-drift comparator
4. Temperature-compensated precision +10V reference

5. High-impedance buffer follower
6. Gated clock and digital control circuits

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, $\pm 1\text{mV}$ by active laser trimming of the thin-film resistors which determine the closed-loop gain of the op amp.

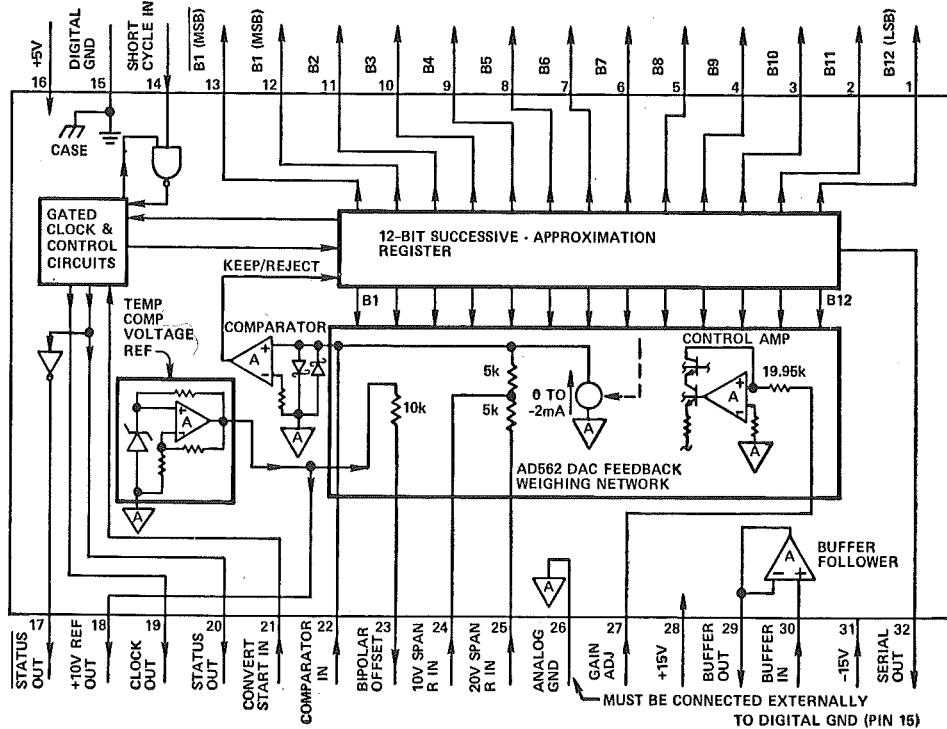


Figure 46. AD572 functional diagram & pinout.

The DAC feedback weighing network comprises a proprietary 12-bit analog current switch chip and silicon-chromium thin-film ladder network (separately packaged as the AD562 12-bit D/A converter). This ladder network is active laser-trimmed to calibrate all bit-ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit-output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 47. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied

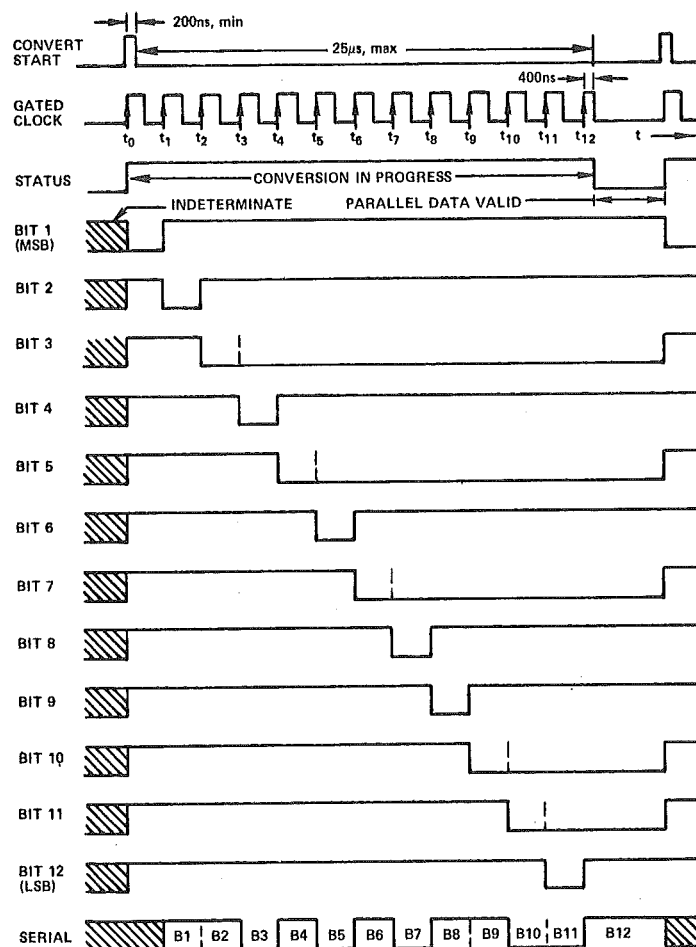


Figure 47. Timing diagram (binary code 110101011001)

to the gated clock, permitting it to run through 13 cycles. All SAR parallel-bit and STATUS flip-flops are initialized on the leading edge, and the gated clock-inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0 , B_1 is reset and B_2 - B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2 , the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12} . After a 400ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 48).

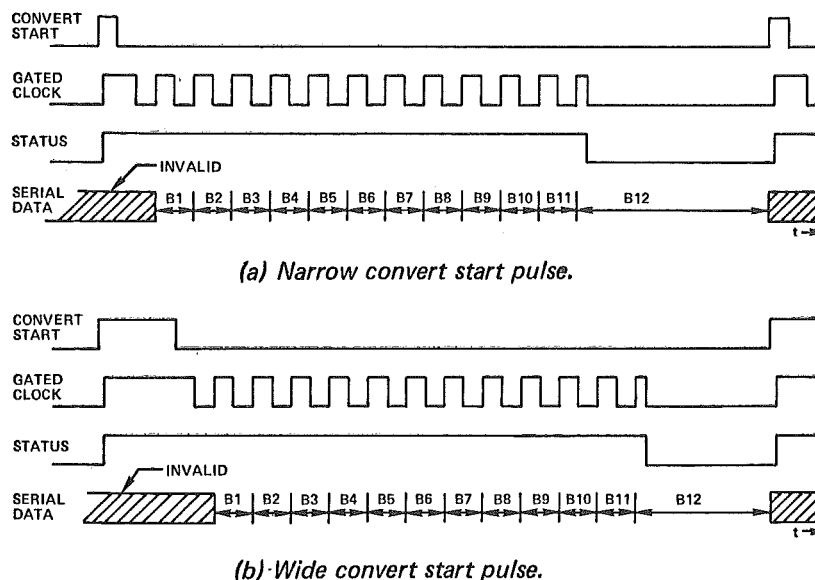
Incorporation of this 400ns delay period guarantees that the parallel (and serial) data are valid at the logic "1" to "0" transition of the STATUS flag, permitting parallel data-transfer to be initiated by the trailing edge of the STATUS signal.

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement bipolar, depending on whether Bit 1 (pin 12) or its logical inverse BIT 1 (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

APPLICATIONS

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 49, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that e_o S_H is in steady-state before conversion is initiated. This insures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 50.



Digital Gain Control: Figure 51 shows a method of adjusting the AD572 gain digitally, using an 8-bit DAC. The 100Ω GAIN ADJ potentiometer is replaced by a 15Ω fixed resistor. This biases Full-Scale high by approximately $35\Omega/20,000\Omega = +0.18\%$ of FSR. The AD559 has a large positive compliance voltage which permits its Current Output, pin 4, to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage-reference, connected through a 1kΩ resistor to Reference Current input (pin 14). The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current $-2.5\text{mA} \times 15\Omega/20\text{k}\Omega = 1.88\mu\text{A}$, or $-1.88\mu\text{A}/500\mu\text{A} = -0.38\%$ of FSR; this permits a digital gain adjustment range of approximately $\pm 0.2\%$ FSR from nominal.

CONCLUSION

As we noted at the beginning of this chapter, it would address itself to a discussion of *converter* microcircuits. As we also noted, it should not be forgotten that converter microcircuits from Analog Devices are accompanied by a panoply of supporting linear IC's – references, sample-holds, multiplexers and CMOS switches, resistance networks, V/f converters, op amps, and instrumentation amplifiers – employing similar technologies (as appropriate) to those used for converters.